A Novel Methodology for Reducing the Flash Memory Development Cycle

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The development cycle for flash memory technology and design architecture is quite long. To be competitive, the cost per unit area has to be minimized while keeping the manufacturing yield at an economically acceptable value. If our objective is then to maximize the number of good chips per wafer, there are two important components of the design optimization, namely derivation of optimal layout design rules and redundancy scheme (including error recovery/correction algorithms and circuitry). Our approach proposed in this paper enables these tasks to be accomplished earlier in the technology and product development cycle, and allows a shorter overall time to market.

Our methodology is based on predictive modeling of the raw (virgin) and redundant yield. In the past, critical area analysis has been used successfully to estimate product yield loss due to random defects. Such "macro" yield predictions provide limited insight, however, into the physical failure mechanisms with the greatest actual (or potential) impact on product yield. To help bridge this gap between process-specific defect mechanisms and product-specific failure modes, this paper presents a modeling methodology for defect-driven yield loss which offers "microscopic observability" of physical failure mechanisms. The key step in our methodology is a prediction of "micro-yield loss events" which correspond to selected "failure event signatures" observed in bitmap and binmap test data. Examples of micro-yield loss events include: two, three or more adjacent row shorts; two, three or more adjacent column shorts; row/column shorts and lack of contact to the cell.

A detailed yield model has been developed for calculation of yield losses per failure mode per defect type. This yield model is formulated in terms of critical areas per defect type, and defect density and size distributions. For technologies with the design rules of 0.25 μm and below, a layout printability simulation is performed first to obtain more realistic representation of the actual geometries on the wafer. Critical areas leading to micro-yield loss events are computed using geometrical oversizing and categorizing resulting polygon overlaps according to the participating electrical nodes. Since each critical area polygon is categorized into a single event class, all micro-yield predictions are guaranteed to be statistically independent. Uncategorized critical areas are combined to form an "unrepairable event" class. The style and extent of micro-yield loss events selected for modeling is determined by the redundancy scheme of the memory device. Only those events which may be repairable must be modeled individually.

The next step in the methodology forms a chip-level yield prediction by combining a hierarchy of micro-yield loss events. Chip, block and cell level repair constraints and resources, as well as unrepairable interactions between these levels determine the model hierarchy.

The final step of the methodology targets absolute calibration of the yield models using in-line inspection data. Just as with macro-yield predictions, micro-yield predictions require careful size-distribution analysis of in-line inspection data in order to accurately predict end-of-line yields. Data for such a calibration could be obtained from the early test chips that are being used for verification of cell designs (e.g., the cell array test chips with minimum peripheral circuitry). After the calibration step is performed, the resulting yield model can be used for derivation of optimal design rules, local optimization of array and periphery layout, and evaluation of redundancy and ERC needs. Moreover, defect targets per layer and type can be derived and transferred to the volume production fablines.

In this paper, we will present examples of yield impact prediction for the dominant defect types found in the state-of-the-art flash memory processes. We will also present an evaluation of the redundancy scheme effectiveness for an industrial design. Finally, we will demonstrate an impact of the design rule changes on the raw and redundant yield.

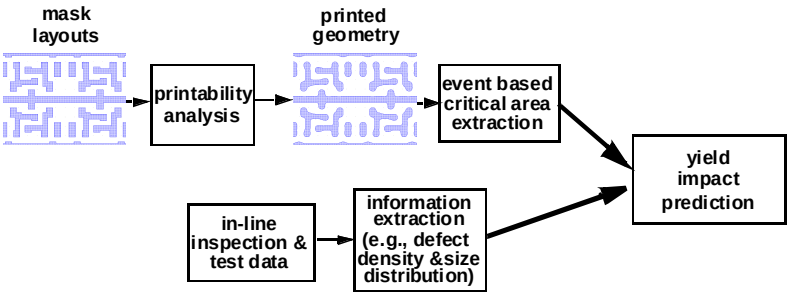

Figure 1. Yield impact assessment methodology based on failure event critical area and defect attribute extraction.

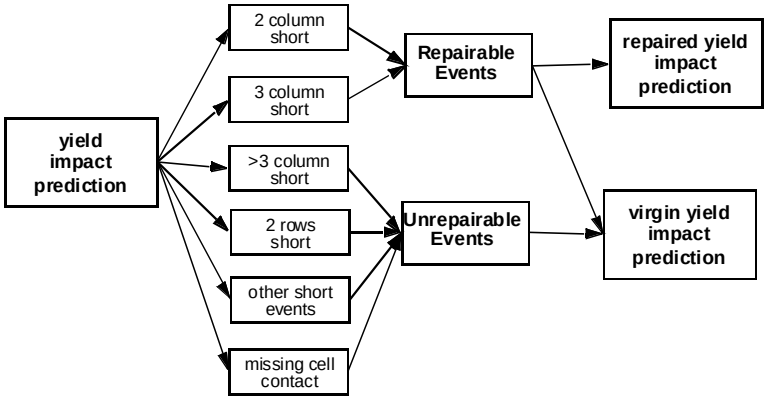

Figure 2. Examples of micro-yield events and yield model hierarchy.

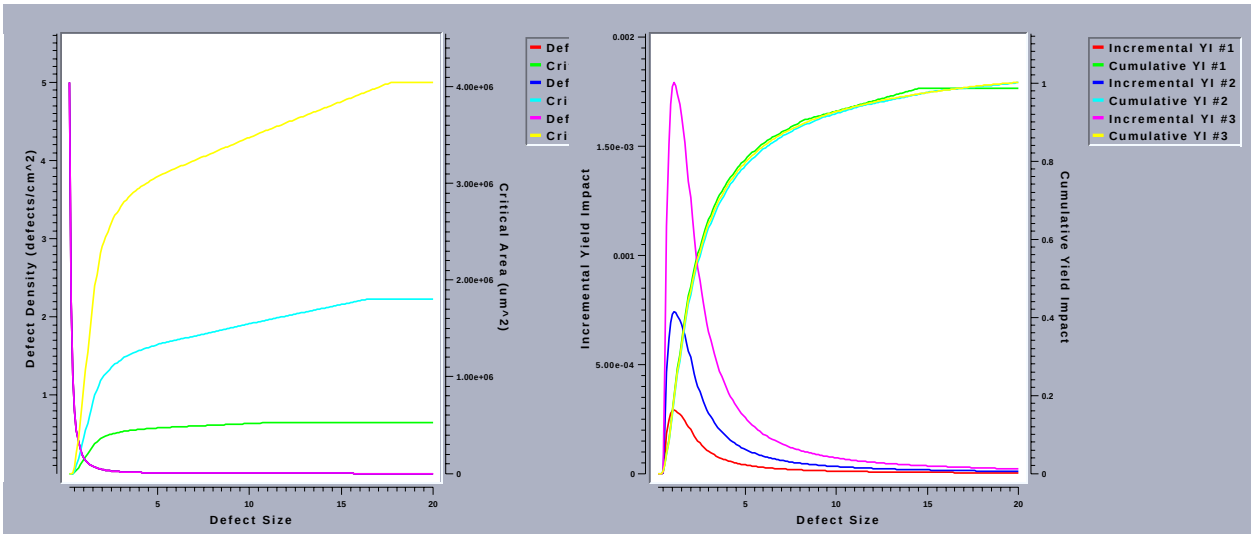

Figure 3. Critical area and defect yield impact curves |for different cell/array designs and repair schemes.