An Asymptotically Constant, Linearly Bounded Methodology for the Statistical Simulation of Analog Circuits Including Component Mismatch Effects

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Abstract: This paper presents a new statistical methodology to simulate the effect of both inter-die and intra-die variation on the electrical performance of analog integrated circuits. The main feature of this methodology is that it accounts for device mismatch by using a number of variables that is asymptotically constant in the limit of perfectly matching devices, and is typically close to the number of independent process factors normally used to account for inter-die process variations only. A unified model of process variation allows the effects of each source of variation and their joint impact to be estimated, thus providing designers more accurate analysis and variance optimization capability. State-of-the-art application examples demonstrate the accuracy and efficiency of this approach.

1.0 Introduction

Accurate matching of the electrical properties of active and passive elements is fundamental for functional and parametric performances of analog and mixed-signal IP blocks, such as OPAMPs, D/A and A/D converters, PLLs, etc. [1]. Achieving target functional and parametric yield of analog and mixed-signal components frequently represents a major bottleneck for the global time-to-volume performance of complex VLSI systems [2]. Therefore, a considerable effort has been devoted to the analysis and modeling of matching properties of electronic devices, such as the original work of Pelgrom et al. [3] and Michael et al. [4], aimed at deriving a suitable model of intra-die MOSFET variance as a function of device size, layout distance and orientation. Although these models have become very popular, their direct application in the context of electrical circuit simulation remains awkward for two main reasons.

First, they model the matching properties of MOSFET "*macro*" characteristics, such as V_{Th} or I_{DSAT}, that are only indirectly related to the actual "*low-level*" parameters of most widely used compact SPICE simulation models, such as BSIM3v3 [5] or MOS9 [6]. Therefore, a non-trivial inverse modeling process must be applied to extract the proper covariance structure of low-level SPICE model parameters corresponding to the available matching characterization data for these macro parameters.

Second, applying a device level mismatch model to the statistical simulation of electronic circuits requires the assumption that every matched device is described by a different set of low-level device parameters, each associated with a corresponding random variable (RV) [7],[8],[9]. The variance of the relevant circuit performance parameters can then be estimated via Monte-Carlo analysis [11]. This process requires the generation of a sequence of correlated vectors of random numbers, and the evaluation of the circuit performance corresponding to each random vector instance either by directly using SPICE or via RSM macro-modeling. The dimensionality of the corresponding RV space can be very large when the simultaneous variation of all matched n-tuples of devices is considered.

In this paper we present a new methodology that allows statistical simulation of a large number of devices subject to intra-die variability. This is accomplished by adopting a unified model of inter-die and intra-die variation, which in the worst-case adds a number of variables that increases only linearly with the number of matched components. However, typically this approach results in a much smaller number of additional random variables to account for intra-die variation.

2.0 Previous Work

The problem associated with the large dimensionality of the mismatch simulation task has not yet been properly addressed in the existing literature. The σ-space approach described in [7], which can be proven to be equivalent to the Choleski factorization technique used in [9], requires $\sum_{j=1}^{nd} (N(m_j) - 1) \times N(p_j)$ different RVs, where, $N(m_j)$ is the number of matched devices of type j, $N(p_j)$ *is the* number of independent process factors used in the model of the j th device type, and nd is the number of different devices in the circuit.

The empirical approach of Guardiani et al. [8], has an even greater complexity, and can be only applied to very simple circuits. Conti et al. [10] proposed a method based on the experimental characterization of a parametrized auto-correlation function for the relevant process parameters described as spatial stochastic processes. The auto-correlation function is then used to derive a symbolic formula for the system covariance matrix as a function of the layout parameters. Therefore, the complexity of this methodology is also proportional to the same number of variables as the σ–space approach, however this technique is compatible with the statistical simulation methodology described in this work, and can be used to replace our covariance modeling methodology.

3.0 Unified Representation of Process Variation

Our approach constructs an efficient representation of both inter-die and intra-die variation to analyze the joint impact of these sources of process variation on a design. The impact of manufacturing variations on a component is typically represented by estimating the distribution of SPICE model parameters for that component [12]. A statistical SPICE model that represents both inter-die and intra-die variations has to account for two types of correlation: between model parameters and between matched components. The correlation between model parameters arises because most commonly used SPICE models utilize non-independent parameters. The correlation between different components on the same die arises because of intra-die process variation.

Both the inter-die and intra-die correlation can be represented in a single correlation matrix. Given n matched components $(C_1,...,C_n)$ and a SPICE model for each component with m parameters

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$(p_1,...,p_m)$, a straight-forward implementation would construct a $nm \times nm$ correlation matrix:

$$\begin{bmatrix} 1 & \rho_{11,12} & \cdots & \rho_{11,nm} \\ \rho_{12,11} & 1 & \cdots & \rho_{12,nm} \\ \cdots & \cdots & \cdots & \cdots \\ \rho_{nm,11} & \cdots & \rho_{nm,n(m-1)} & 1 \end{bmatrix} \quad (1)$$

where the rows and columns are $T_i p_j$, representing parameter j for transistor i. The element $\rho_{ij,kl}$ represents the correlation between $T_i p_j$ and $T_k p_l$.

This representation is computationally very expensive: the matrix grows as $O(nm \times nm)$. Two simplifications are possible by using principal component (PC) decomposition. The first simplification is the use of PCs to represent the correlation between the model parameters and the second simplification is the use of PCs to represent the correlation between the matched devices.

3.1 Inter-die PC Decomposition

PC representation expresses a set of correlated RVs in terms of a set of independent RVs [13]. This is obtained by applying a congruence transformation of the form: $\Gamma\Sigma\Gamma^T = \Lambda$ to the covariance (or correlation) matrix Σ, such that Γ is an orthogonal matrix and Λ is diagonal matrix, its elements λ_{ii} are the eigenvalues of the covariance matrix. An important property of PC decomposition is that:

$$\sigma_q^2 = \left(\sum_{i=1}^{q} \lambda_{ii} \right) \Big/ \left(\sum_{i=1}^{n} \lambda_{ii} \right) \quad (2)$$

represents the fraction of the variance explained by the first q PCs. Use of PCs to represent correlation in the model parameters is well known [14]. By replacing the model parameters $(p_1,..., p_n)$ by PCs $(f_1,..., f_k)$ in the Eq. (1) one gets a $nk \times nk$ size matrix, where typically $k \ll m$. The reduction in the matrix size stems from the application of a suitable threshold filtering algorithm based on Eq. (2). However, further simplifications are possible because using PCs instead of model parameters makes the correlation matrix very sparse. Because the PCs are independent, the correlation between different factors for the same component is zero, i.e., $\rho_{il,im} = 0$ for $l \neq m$. Moreover, since the PCs are considered to represent independent sources of variations, correlation between different parameters on different transistors is also taken to be zero., i. e., $\rho_{ij,kl} = 0$ for $i \neq k$ and $j \neq l$. This leaves only one set of non-zero entries in the correlation matrix: between the same factor for different matched components, i. e., $\rho_{il,jl}$.

3.2 Intra-die PC Decomposition

The correlation matrix is further simplified by using a second level of PC decomposition, replacing a PC of the original model, e. g., f_j, by a linear combination of a set of second-level PCs representing the intra-die variation. The result of the second PC decomposition is a unified representation that captures both the correlation between the model parameters and the matched components. Moreover, the transformation maintains the correlation between the model parameters, because the RV for each original PC is replaced by an equivalent with the same mean and variance. The second level PCs transformation adds, at worst, n new PCs, resulting in a total of $n \times k$ PCs. Since the statistical SPICE model is independent of the application, the number of PCs k is fixed, and usually $k \ll m$, where m is the number of model parameters. This results in a mismatch simulation method that adds only $O(n)$ new RVs for a circuit with n matched components.

An advantage of our approach is that in practice the number of factors required is scarcely the $n \times k$ factors required in the worst case. This happens for two reasons. First, not all k PCs required to capture the correlation of the model parameters are necessary for representing mismatch. Usually, a much smaller number of variables are required. Second, because the amount of mismatch is typically very small, we expect the correlation matrix to be in general characterized by a small number of dominant eigenvalues. Therefore, using Eq. (2) the variance of the system can be approximated well by using a small number of PCs compared to the worst-case n.

For example, in the asymptotic case of perfectly matched devices, this method automatically produces only one PC (corresponding to the dominant eigenvalue) for each independent process factor, resulting in no increase in the number of RVs. In the intermediate situations between the worst-case and the asymptotic case, our approach provides an obvious approximation scheme where a small number of PCs can be selected to accurately approximate the correlation between the components.

4.0 Statistical SPICE Models with Mismatch

Mismatch characterization typically does not produce the correlation between PCs of a statistical SPICE model. Usually, the result of mismatch characterization is a set of coefficients for a mismatch model of device performance. For example, MOS transistor mismatch characterization often results in the coefficients of a Pelgrom-style model for threshold voltage (V_{Th}) and saturation current (I_{DSAT}) or the transistor gain-factor (k')[1]. To utilize this information in the representation described above it must be converted into correlation between PCs of the statistical SPICE model.

The procedure for determining the unified statistical representation starts with a statistical SPICE model for correlation between model parameters. A subset of the PCs of this model is selected for representing component mismatch. The selection is based on two considerations: the device characteristics for which mismatch has been characterized, and the weightings of the different PCs in the equation for each SPICE parameter that impact these device characteristics. For example, if mismatch characterization has been performed for threshold-voltage and gain-factor of long-channel MOSFETs, then PCs that have the most impact on the VTH0 and U0 (mobility) parameters of the BSIM3v3 model are selected. Once the PCs of the model without mismatch have been selected, a numerical optimization is performed to find the correlation between these factors in order to obtain the measured mismatch in device characteristics.

Each optimization results in the correlation of the selected PC for one set of device geometry and layout parameters. Repeating this procedure for different geometries and layout distances results in a set of correlation values that are either fit with an interpolating function or represented in a look-up table. This procedure results in a model of PC correlation as a function of device geometry and layout. The step of modeling PC correlation as a function of device geometry and layout is performed only once for a particular technology and layout style.

5.0 Implementation

The statistical simulation technique presented here has been implemented as part of the Circuit Surfer statistical design environment [15]. This environment supports many tasks typically required for analog and mixed-signal design for manufacturability, such as statistical simulation, sensitivity analysis, response surface modeling, and circuit optimization for manufacturability. Mismatch simulation is implemented in this environment as an annotation of the circuit netlist to specify the matched components and annotations to the statistical SPICE models to include the effect of mismatch. The annotated netlist and SPICE models are used to derive a separate statistical SPICE model for each component using the two-level PCA described in Section 3.0. The modified netlist forms the input to Circuit Surfer. This implementation enables all the capabilities of statistical design for mismatch analyses such as variable screening, response surface modeling and Monte-Carlo using mismatch factors, and optimization of a design to reduce its mismatch sensitivity.

6.0 Application Examples

Two designs were chosen to demonstrate our methodology; a low voltage OPAMP and D/A Converter. These topologies were implemented based on their continued significance in low voltage VLSI signal processing applications and their performances sensitivities to device mismatch characteristics.

6.1 Low Voltage OPAMP

The OPAMP is of the 2-stage rail-to-rail class-AB architecture shown in Figure 1 which employs a constant-g_m input stage with tail current control [16],[17].

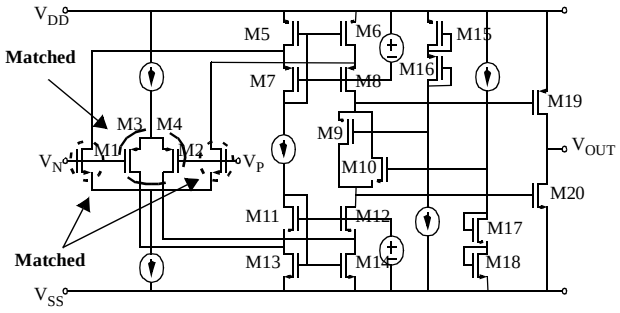

Figure 1: Low Voltage OPAMP Schematic

The commonality of complimentary input stages in today's designs makes this topology ideal for exploring the effects of mismatch on offset voltage (*Vos)* given both NMOS and PMOS mismatch effects. In addition, low voltage design examples such as this help exploit the increasing dependence of proper signal resolution on low *Vos*. A Pelgrom model for the mismatch in the threshold voltage and gain factor of long-channel transistors was available for this class of technologies. For the matched NMOS pair M1-M2, the model specifies $\sigma(\Delta(Vth)) = 2mV$ and $\sigma(\Delta(k')) = 0.7\,\%$. For the PMOS pair M3-M4, the mismatch was: $\sigma(\Delta(Vth)) = 1.5mV$ and $\sigma(\Delta(k')) = 0.45\,\%$. This mismatch specification was transformed to correlation between the PCs of the statistical SPICE model for this technology and a unified statistical SPICE model was derived for the matched pairs as described in Section 3.0. Only three additional factors, of a total of nine factors, were sufficient to represent intra-die variation for the two pairs of matched transistors. The impact of mismatch on this design is shown in Table 1.

Table 1: Impact of Mismatch on OPAMP (10,000 sample Monte-Carlo)

Performance	Without Mismatch		With Mismatch	
	Mean	std. dev	Mean	std. dev
Vos (mV)	-1.803	0.09627	-1.802	0.7216

Two sets of Monte-Carlo simulations were performed, one using only the inter-die model and the second using the unified model. As expected, this design shows that *Vos* is extremely sensitive to mismatch. By quantifying the exact impact of mismatch our method allows an accurate assessment of manufacturability of this topology. It also shows that parametric yield estimates can be overly optimistic for designs sensitive to mismatch if mismatch effects are not accounted for in statistical simulation or worst-case models. Figure 2 shows the distribution of *Vos* with and without mismatch. The overlay illustrates the 7X increase in the offset voltage standard deviation. Without the ability of efficient and accurate mismatch analysis the impact on parametric yield due to this increase would be missed.

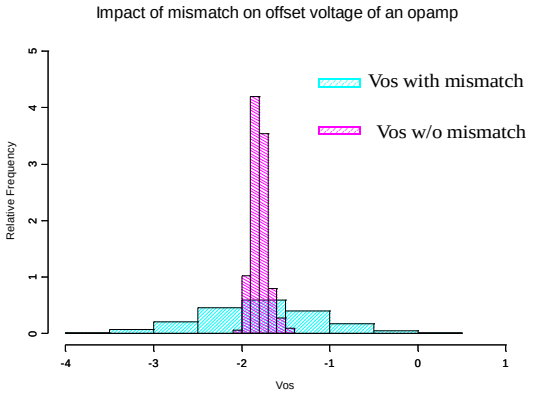

Figure 2: Distribution of Vos with and without mismatch

6.2 D/A Converter

The D/A Converter shown in Figure 3 uses a binary weighted current implementation with eight-bit resolution. The output current is summed via current switching and output to a linear I-V converter [18]. Data converter non-linearity is a measure of the error induced by the converter and it is sensitive to the matching between the transistors comprising the ratioed current source.

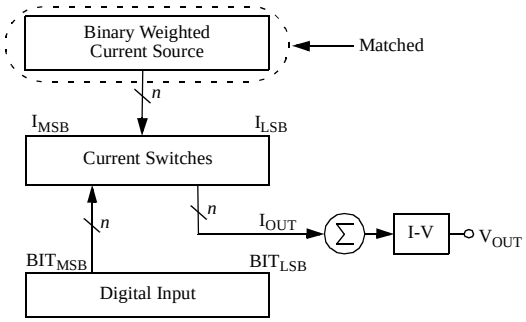

Figure 3: D/A Converter schematic

Simulation with and without intra-die variation was carried out as described for the OPAMP. The mismatch effects were examined for the binary weighted current source identified in Fig. 3. Specifi-

cally, the analog output was tested for differential non-linearity (DNL), defined as the deviation of each set of adjacent steps at the analog output from their ideal value (1 LSB). Here, we have defined the performance specification to be +/- 1/2 LSB.

Table 2: Impact of mismatch on D/A Converter (10,000 sample Monte-Carlo)

Performance	Without Mismatch		With Mismatch	
	mean	std. dev	mean	std. dev
DNL (LSB)	-0.176	0.086	-0.198	1.155
Yield	100%		34%	

The results of statistical simulation with and without intra-die effects are shown in Table 2. Intra-die variation causes the standard deviation of DNL to increase by a factor of 13. Such a large increase in the increment causes large changes in the linearity of the D/A Converter. As in the previous example, including intra-die effects is vital to get accurate estimation of circuit performance variability, but since the circuit's performance for this topology depends upon the pairwise matching of eight different transistors, a complete statistical simulation using a standard methodology would entail running a Monte-Carlo experiment with large number of correlated RVs.

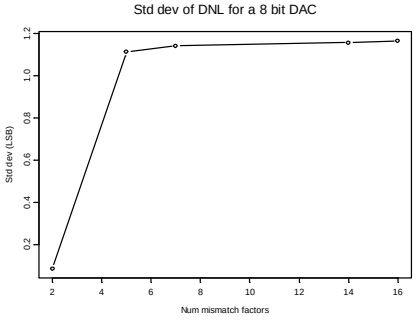

Figure 4: Mismatch simulation with reduced factors

For example, a circuit with eight matched transistors and 7 to 12 independent sources of process variation (typical of advanced CMOS processes) requires the generation of a sequence of correlated random numbers for as many as 96 different RVs. Several thousand SPICE evaluations would be required to stabilize the Monte-Carlo results for such a high-dimensional system. However, as illustrated by the graph in Figure 4, our method has the ability to simulate the impact of intra-die variation accurately with a small number of additional mismatch factors. This figure shows the standard deviation of DNL versus the number of additional factors employed for mismatch simulation. In fact, although in the worst case our technique would require 18 additional RVs, by applying the screening methodology described in Section 3.0, it was possible to model very accurately the impact of intra-die variability on the D/A Converter with only two additional variables. This result makes the simulation of mismatch applicable to an inherently larger set of matched transistors; a requirement as supply levels and feature sizes continually decrease and previously negligible device effects become increasingly significant.

7.0 Conclusion

This paper presented a new methodology for constructing combined models of both local and global variation by applying PC decomposition twice to an $nm \times nm$ correlation matrix which expresses the inter-die and intra-die variability of MOS transistors. The models produced are simpler to use than those generated by other methods because the parameters of the models are defined in terms of SPICE model parameters and the number of variables required is relatively small. The number of variables lies close to the number of independent process factors and is asymptotically constant in the case of perfectly matched devices. Examples were provided to support the case that the parametric yield of common analog circuits cannot be estimated with any confidence if the effect of mismatch is ignored.

8.0 References

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