

# Circuit-Device Co-design for High Performance Mixed-Signal Technologies

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**Abstract:** System-on-Chip designs require low cost integration of analog and digital blocks. Often, the analog requirements are not considered sufficiently early in the device design cycle, resulting in devices that are suboptimal for the analog components. This paper presents an innovative methodology for deriving comprehensive device specifications based upon a set of Figure-of-Merit circuits which account for both analog and digital requirements. By utilizing these specifications for device design, a more efficient codevelopment of mixed-signal processes, libraries and products is possible. The methodology is illustrated with an example based upon an advanced 120nm CMOS technology.

## I. INTRODUCTION

Low cost integration of baseband and RF analog functions with high performance logic is mandatory for System-on-Chip (SoC) applications [1]. Two deep-submicron (DSM) technology trends add to the difficulty of such integration. First, voltage scaling and tighter noise specifications increase the challenge of designing the analog IP blocks. Second, CMOS device optimization is typically driven by specifications that focus on increasing drive ( $I_{dsat}$ ) and reducing off-state current ( $I_{off}$ ), while minimizing junction and overlap capacitances. Analog device characteristics, such as  $g_m$ ,  $g_{ds}$ , noise, matching, are often either ignored or deferred to subsequent refinement steps. Poor analog characteristics may result in either suboptimal performances or expensive redesign of the analog blocks.

This paper describes a novel methodology for deriving a set of transistor design specifications based upon performances of a library of Figure-of-Merit (FOM) circuits. These specifications form the basis for obtaining device structures required to achieve transistor characteristics optimal for both analog and digital design. Transistor optimization for both analog and digital requirements improves the performance of the analog blocks while maintaining digital circuit speed. This methodology is demonstrated with an example of improving the analog performance of an advanced 120nm CMOS logic technology.

## II. CO-DESIGN METHODOLOGY

The purpose of the co-design methodology is to take circuit and system level considerations into account during device design. Our methodology for accomplishing this involves four main components:

1. A set of FOM circuits to estimate the impact of technology choices on the target applications.

2. A representation of the space of allowable device designs suitable for circuit simulation. This is accomplished by developing a *parameterized SPICE model*.

3. A search and optimization procedure to identify the device designs that exhibit the optimal trade-off with respect to the FOM circuits.

4. Inverse modeling to define the structure and doping of the device that achieves the device performance identified during the optimization.

### A. FOM Circuit Library

The circuits in the FOM library are simple, canonical circuits that capture the suitability of a technology for a particular class of applications. The simplest and most well-known example of a FOM circuit is a ring-oscillator; the propagation delay ( $t_{pd}$ ) of a ring-oscillator is a good indicator of the suitability of a transistor technology for high-speed digital applications. For SoC applications circuits representative of a technology's performance for analog applications are also included.

Two kinds of FOM circuits are included in a FOM library: generic and application specific. Generic circuits are intended for a platform technology with wide range of applications. Examples of such FOM circuits and their respective perfor-

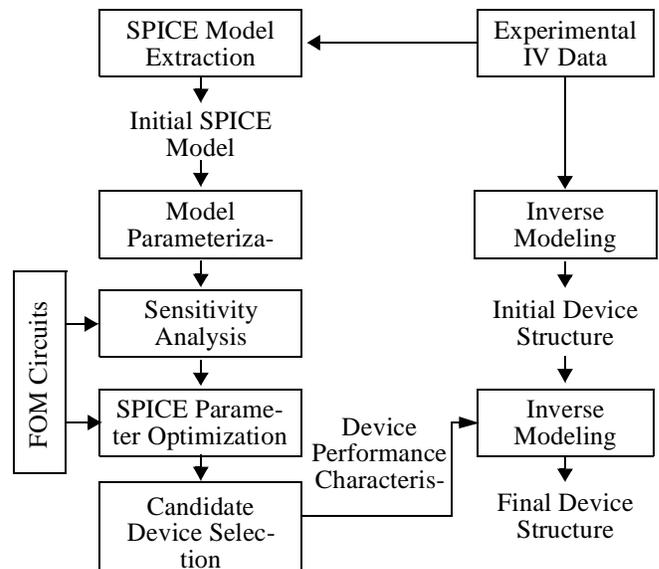


Fig. 1. Design Flow for Device Optimization Based on FOM Circuits

mances for SoC applications include: ring oscillator for digital applications, simple operational transconductance amplifiers (OTA) whose AC/DC characteristics are representative of most amplifiers; current mirrors to estimate the effects of output conductance; and a MOS switch for switched capacitor applications. In addition to nominal performances like  $t_{pd}$ , gain ( $A_v$ ), 3dB frequency, etc. the variability transmitted by process variation to the circuit performance can also be monitored via the standard deviation of these performances. If the space of device designs included options that change the device mismatch, these can be monitored with the current mirror and OTA as well. Application specific circuits can be added to the library for situations where the technology is to be optimized for a certain class of applications. For example, data-converters can be included for technologies intended primarily for digital-signal processing and communications applications.

### B. Parameterized SPICE Models

There are two methods to simulate the impact of device design on circuit, mixed-mode device and circuit simulation, and development of parameterized SPICE models. Mixed-mode simulation has the advantage of not requiring a SPICE level representation of the design but is limited in the size of the circuits that can be easily simulated. The circuits in the FOM library have more transistors than can be readily simulated with mixed-mode simulation. One method of addressing this problem is through the development of parameterized SPICE models.

Parameterized SPICE models represent the device design space by allowing SPICE parameters to be functions rather than single values. The output of these functions is the value of the SPICE parameter and the input to the functions and the form of the function define the space of allowable device designs. For example, a parameterized model for a common SPICE parameter for long channel threshold voltage ( $V_{TH0}$ ) may have the form:  $V_{TH0} = V_{TH0_{nom}}(1 + \alpha)$ , where  $V_{TH0_{nom}}$  is the value for the nominal value of the parameter and  $\alpha$  represents the amount by which the long-channel threshold voltage can be changed by device design.

Most common SPICE models are over parameterized so it is essential to ensure that the parameterized SPICE models only permit feasible devices. This requires that the proper correlation is maintained between model parameters. There are two approaches for accomplishing this goal. First, if a silicon or calibrated simulation experiments over the range of interest are available, then the change in the key SPICE models parameters can be extracted for each condition in the experiment design (DOE). The function connecting the process parameters to the model parameter can be estimated empirically by fitting a response surface[5].

The second approach is to initially place a set of constraints between model parameters and then allow the remaining model parameters to vary freely. For example, the well-know analytic equation connection gate-oxide thickness (TOX), peak channel concentration (NCH), and long channel threshold voltage ( $V_{TH0}$ ) is used to allow only two of the variables,

say (TOX) and NCH to vary and the other variable is derived from known analytic relationship. Since this approach can result in infeasible devices, a measure of distance from the initial device is used as an indicator of device feasibility; devices with parameter values close to the initial device are preferred over those with larger distance. An additional step of inverse modeling is performed to find feasible devices that come closest to the optimized device characteristics estimated by this approach. For the application reported in this paper, 26 BSIM3v3 parameters are allowed to vary independently by up to 30% during optimization.

### C. Device Design by Inverse Modeling

Inverse modeling techniques extract structure and doping information about a semiconductor device from its measured electrical behavior [2]. Since electrical measurements are readily available, inverse modeling is a very effective technique for structural characterization of DSM technologies where direct physical measurements are extremely expensive, inaccurate, and time consuming. We solve the problem of uniqueness associated with inverse modeling by utilizing a large number of device measurements: DC IV curves at different back biases ( $I_{dsat}$ - $V_g$ ,  $I_{dlin}$ - $V_g$ ,  $I_d$ - $V_d$ ) and AC performance parameters ( $C_{js}$ ,  $C_{jd}$ ,  $C_{gd}$ ,  $C_{gs}$ )

## III. APPLICATION EXAMPLE

The co-design methodology described here was applied to improve the analog characteristics of transistors from an advanced 120nm CMOS logic technology. Analog performances were monitored using operational transconductance amplifiers (OTAs), current mirrors and MOS switches. Digital performances were monitored using multiple fan-out ring oscillators. The objective of the optimization was to improve leakage and output conductance while maintaining speed (i.e. reduce  $I_{off}$  and  $g_{ds}$ , while maintaining  $t_{pd}$ ). Table 1 compares both the device level and circuit level performances of the initial and optimized transistors. Note the 10-15% reduction in  $g_{ds}$  and the reduction of  $I_{off}$  to bring it within the typical  $1nA/\mu m$  requirement. This was achieved by only a 3% increase in  $t_{pd}$ . Fig. 2 and Fig. 3 compare  $I_d$ - $V_d$  characteristics of the optimized and inverse-modeled devices..

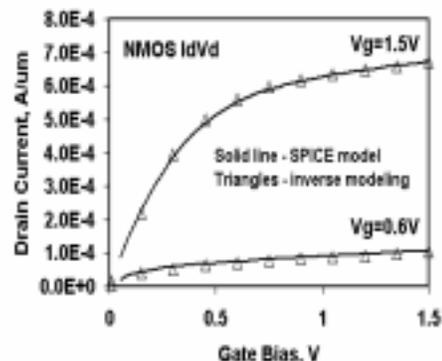


Fig. 2. Drain Curves of Optimized NMOS

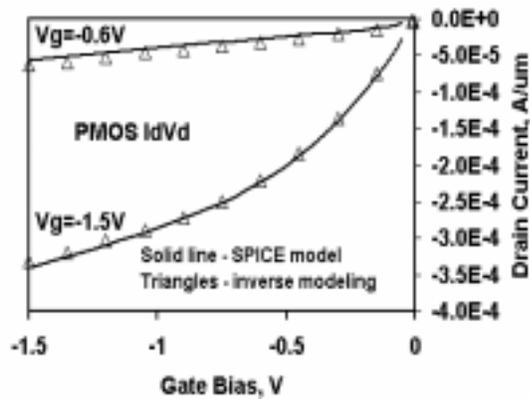


Fig. 3. Drain Curves of Optimized PMOS

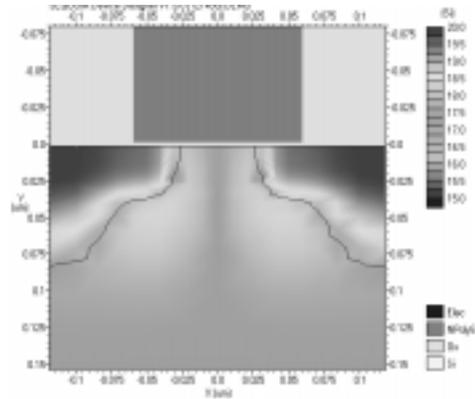


Fig. 4. Optimized Device Structure for NMOS

TABLE I  
Optimized Circuit/Device Performance

Circuit/Device	Parameter	Initial	Optim.	%
NMOS	Vtsat (mV)	268	286	+7%
	Vtlin (mV)	400	397	-1%
	Idsat ( $\mu\text{A}/\mu\text{m}$ )	692	673	-3%
	Ioff ( $\text{nA}/\mu\text{m}$ )	1.43	0.877	-40%
	gdsmin ( $\mu\Omega^{-1}$ )	88.6	78.6	-11%
PMOS	Vtsat (mV)	215	250	+16%
	Vtlin (mV)	404	440	+9%
	Idsat ( $\mu\text{A}/\mu\text{m}$ )	340	327	-3%
	Ioff ( $\text{nA}/\mu\text{m}$ )	1.46	0.49	-66%
	gdsmin ( $\mu\Omega^{-1}$ )	96.3	82.6	-15%
Ring Osc.	tpd (psec)	16.7	17.3	+3%
OTA (p-load)	Av (dB)	35.7	33.4	-7%
	f3db (kHz)	363	474	+30%
	Pwr ( $\mu\text{W}$ )	1.19	1.13	-5%
OTA (n-load)	Av (dB)	33.7	33.13	-2%
	f3db (kHz)	254.5	269.5	+6%
	Pwr ( $\mu\text{W}$ )	1.22	1.22	0%

Two dimensional doping distributions obtained from the inverse modeling of both NMOS and PMOS devices are shown in Fig. 4 and Fig. 5

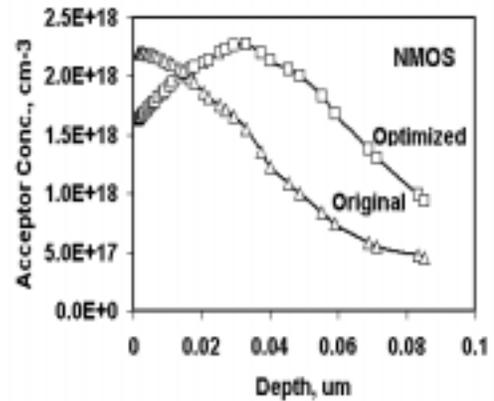


Fig. 5. Vertical Doping Profile at Gate Edge for Optimized NMOS

It was found that the optimized device characteristics could be achieved by adjusting the pocket doping profile of both devices. The net effect of those changes was to make the pocket profile more retrograde in both cases (Fig. 6 and Fig. 7).

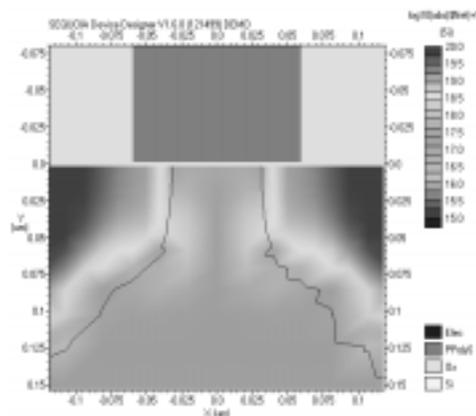


Fig. 6. Optimized Device Structure for PMOS

#### IV. CONCLUSIONS

We presented a new methodology for obtaining transistor specifications and device designs based upon the requirements of a set of FOM circuits. This methodology makes it possible to derive device structures that concurrently optimize both digital and analog circuit design requirements. The method was illustrated by using it to improve the analog performance of an advanced 120 nm CMOS technology originally targeted for digital applications

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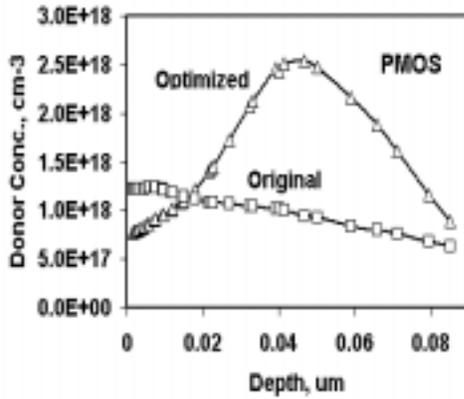


Fig. 7. Vertical Doping Profile at Gate Edge

No other changes to the device structures were required. These results are consistent with [3], which showed that the potential barrier created by a pocket implant at the surface has a negative effect on the device output conductance.