Fast Characterization of Electrical Fails Overlaying to Inline Defect Inspection During 90 nm Copper Logic Technology Development

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***Abstract*—The killer defect re-review method enables a fast identification of front end of line (FEOL) failure modes which is one of the keys to shorten yield learning cycles. This paper describes a combination of overlay techniques of electrical and defect inspection data on one hand and semi-automated defect review of electrically failing structures on the other hand. It was used during the 90 nm copper logic technology development in a joint project of Infineon Technologies Dresden and PDF Solutions and reduced physical failure analysis needs. A comparison of the overall defect density learning rates (including FEOL and copper back end of line limited yields) during 90 nm using this method and 130 nm copper logic technology development is given.**

I. Introduction

It is commonly accepted that fast yield learning is essential during semiconductor technology development to successfully qualify a new technology node and prepare the production ramp. It is therefore no surprise that the yield improvement chapter of the recent update of the International Technology Roadmap for Semiconductors (ITRS 2006) confirmed that tools and methods for short yield learning cycles as well as rapid root cause analysis of yield limiting conditions are needed. Also electrical and physical failure analysis (PFA) for killer defects with high capture rate, high throughput and high precision are demanded [1]. Defect density inspection and defect classification is also playing an increasing role in order to achieve short learning cycles [2], [3]. Because the inspections alone do not catch all yield relevant failure modes and do not measure the yield impact of different defect types, Desineni et al. recently published a method for presenting limited yields calculated on defect density data together with physical failure analysis root causes [4]. They use a special pareto that gives a summarizing message e.g. for the unit process community in order to prioritize yield improvement actions.

One of the tools proven to be successful to provide such a Pareto is the use of short flow test chips. They are commonly accepted to speed up the yield learning [5]. Nevertheless data derived from such test chips are supported by sophisticated failure analysis (FA) methods and thus many efforts are taken to improve the visibility of very small defects that cause a device to fail [6], [7]. Physical failure analyses on saleable products by cross-sectional scanning electron microscopy (SEM) preparation or even by time consuming transmission electron microscopy (TEM) preparation often result in root cause findings that were obvious, if the physical failure would easily be accessible by the standard inline SEM review method which is used in semiconductor mass production. Especially for the front end of line (FEOL) process modules this is difficult to realize as the fail causing defects (killer defects) are covered by the following metal contact module.

This article describes a method where we first searched for the root cause of electrically failing FEOL structures with semi-automatic SEM review and then determined whether further expensive and time consuming cross-section failure analysis was needed. Images of killer defects often provide enough information of an electrical fail so that further physical analysis is not necessary and corrective actions can immediately be started.

II. Killer Re-Review On FEOL Test Chip

A. Schematic Flow

Infineon Technologies Dresden used several test chips in its 200 mm fab for achieving high yield learning rates for the 90nm copper logic technology in a joint project with PDF Solutions. One provided by PDF Solutions was its proprietary

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short-flow Characterization Vehicle® (CV®) test chip, called the Poly CV®, which covered killer defects originating in the shallow trench isolation (STI), poly gate and salicidation modules. Several structures were used to characterize and measure the yield impact of different failure mechanisms which can be caused by process window marginalities and especially by process related defects, such as scratches or particles. Since the Poly CV test chip is electrically tested (using a fast parallel tester) directly after the salicidation process, i.e. without a metal contact module, short yield learning cycles could be achieved for the modules from STI to salicidation.

The analysis of the Poly CV test chip included a dense coverage by defect inspections and defect reviews of both baseline and excursion wafers. An overlay of the coordinates of electrical fails and defects found inline allowed the identification of the main yield detractor process layers. Priorization for further root cause analysis (e.g. defect partitioning) of yield relevant defects was possible by this overlay pareto. The data flow presented in this study includes electrical overlay techniques provided by Poly CV test chip by PDF Solutions and which are described elsewhere in more detail [8].

The so called killer re-review method covered in this article became a powerful method for a fast root cause identification of defect related fails during the 90 nm copper logic technology development at Infineon Dresden and was performed on the Poly CV test chip after the electrical test. The examples of killer re-reviews shown in this section were done on an engineering basis for failing FEOL structure types where yield improvement was primarily necessary or for wafers which showed excursions in limited yield loss. For this first group of examples there was existing an overlay of inline defect inspection data and electrical data but no inline review of the specific defect because it was not part of the review sampling plan used due to the limited review capacity. A second approach was chosen for wafers which had no inline inspection at all (see subsection II. B.). For those the final inline defect scan present in the Poly CV test chip flow was applied after the electrical test. An electrical overlay calculation could be performed on the basis of this data and the killer re-review could then be done. Although some killer images are already found by the overlay calculation between inline review data and electrical data, there is more information that can be easily used for the killer re-review.

The fail coordinates from the overlay analysis were taken to produce review files (standard defect density kla format [3]) which then were used to drive the SEM to the location of the defect for imaging. The killer defect re-review included only electrically relevant defects. It completed the pareto of fail mechanisms known from inline defect review and allowed a fast understanding of the root cause e.g. for excursion wafers for which no images of the inline baseline review were available. It also allowed decisions whether expensive failure analysis (FA) by SEM or TEM cross section preparation was necessary. If obvious failure mechanisms were present (e.g. scratches by oxide CMP or particles masking the structuring of the gate poly, see Fig. 2) FA capacity could be saved for more important defects.

Fig. 1 summarizes the flow of the killer re-review method within the standard PFA flow. Wafers 1, 2, and 3 represent the three flows for a killer re-review. Wafer 1 is inspected and reviewed throughout the short loop process flow of the Poly CV test chip. A killer re-review can be done on a defect caught by the inspection though not reviewed because the review sampling missed the defect which caused a fail. Wafer 2 is inspected on all implemented inspection levels but not reviewed e.g. due to limited review capacity. A killer re-review of wafer 2 will be useful for an excursion wafer or wafers with an electrical baseline issue to be tackled. Wafer 3 is not inspected at all but run on the Poly CV test chip flow to increase the statistical basis of yield measurements. A killer re-review for wafer 3 can be performed after an additional inspection (usually the final inspection prior to the electrical test or a special inspection recipe prepared only for killer re-review purposes). In this case the automated overlay calculation needs to wait for this additional inspection, which is not practicable in a mass production environment but may be appropriate for special engineering topics.

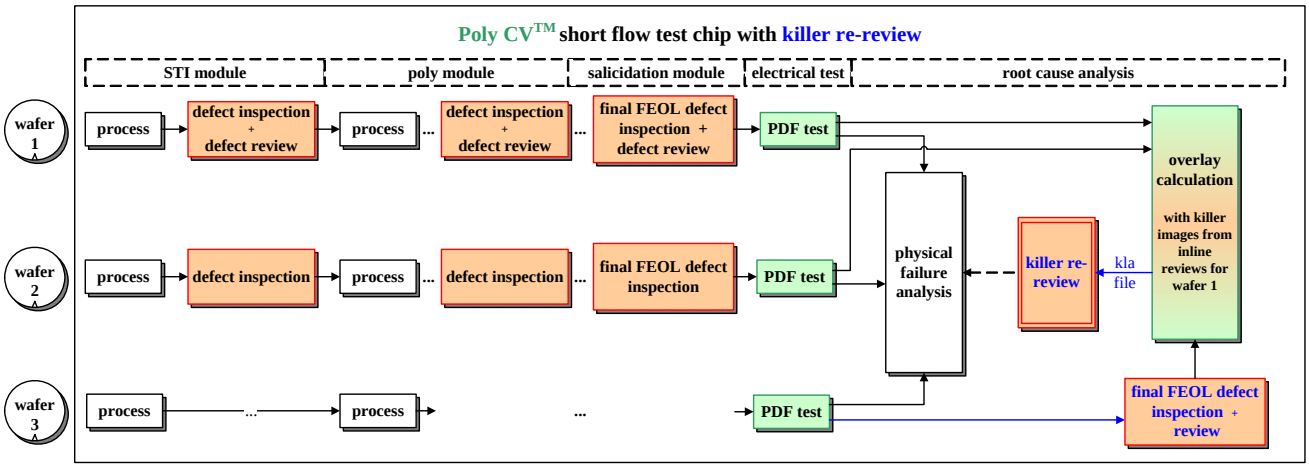

Fig. 1. The killer re-review flow described in this paper. Wafer 1, 2, and 3 represent the three possible ways killer re-reviews of defects originating in the front end of line (FEOL) process modules were successful.

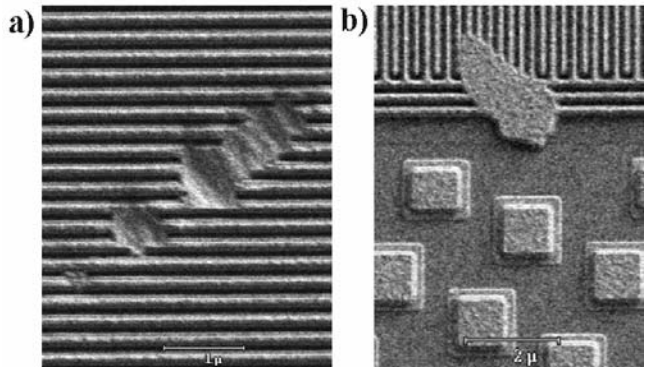

Fig. 2. SEM killer re-reviews of electrical fails (tested post salicidation) overlaying with inline defect density inspections. Cross-sectional failure analyses were not needed because STI oxide CMP scratch (a) or poly gate masking (b) as root causes were obvious. Although the wafer with defect a) was not reviewed (following the flow of wafer 1 or wafer 2 in Fig. 1) and that with defect b) was not even scanned by defect inspections inline (following the flow of wafer 3 in Fig. 1), a fast root cause identification was possible by the killer re-review method. Wafers were processed until salicidation.

B. Killer Re-Review Combined with Inline Defect Review Data

Fig. 3 shows a defect type which was originally not known from the overlay of inline defect review images and electrical fails. The killer re-review allowed a fast identification of this defect type as one already known from inline baseline review.

One of the challenges in the 90 nm logic technology development at Infineon Dresden could be solved by a combined method of analyzing images from the baseline inline review, identifying the same defect type as electrically relevant in a killer re-review, and - because the root cause was not obvious - performing a subsequent FA. One example of this defect type which was present at the defect inspection post gate poly main etch as baseline defect can be seen in Fig. 3(a). Because none of the defects of this type reviewed inline failed, no killer images were found from the overlay calculations. Only a killer re-review (Fig. 3b) revealed that this defect type can cause an electrical fail. The faint shadow could not be assigned to a defect mechanism and thus the decision was taken to perform a prioritized FA by TEM cross section to ensure a significant FEOL defect related yield gain. From the TEM image (Fig. 3c) it could be found that the defect source was in the STI module. Successful experiments for defect reduction in this process module and finally a process change eliminated this defect type and significantly improved and stabilized the FEOL limited yield.

III. Yield Learning Rate

Fig. 4 depicts the defect density learning rate in the 90 nm copper logic technology development compared to that of the 130 nm development. The curves include both FEOL and copper back end of line (BEOL) defect densities. The joint project of Infineon Technologies Dresden and PDF Solutions contributed to a doubling of the yield learning rate.

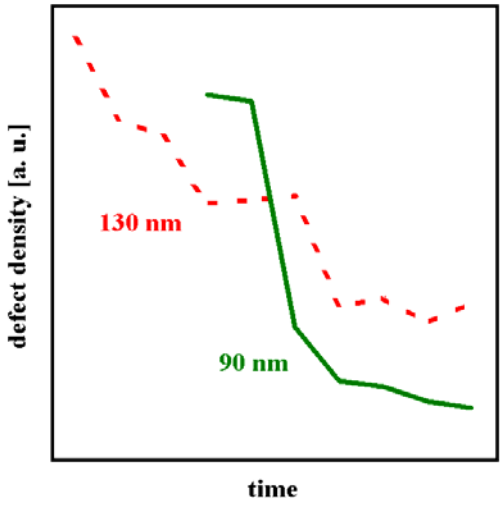

Fig. 4. Learning rate for defect density for 90 nm copper logic technology development at Infineon Technologies Dresden in joint project with PDF Solutions compared to the 130 nm technology ramp. The time axes for both technologies were aligned to the start of the projects.

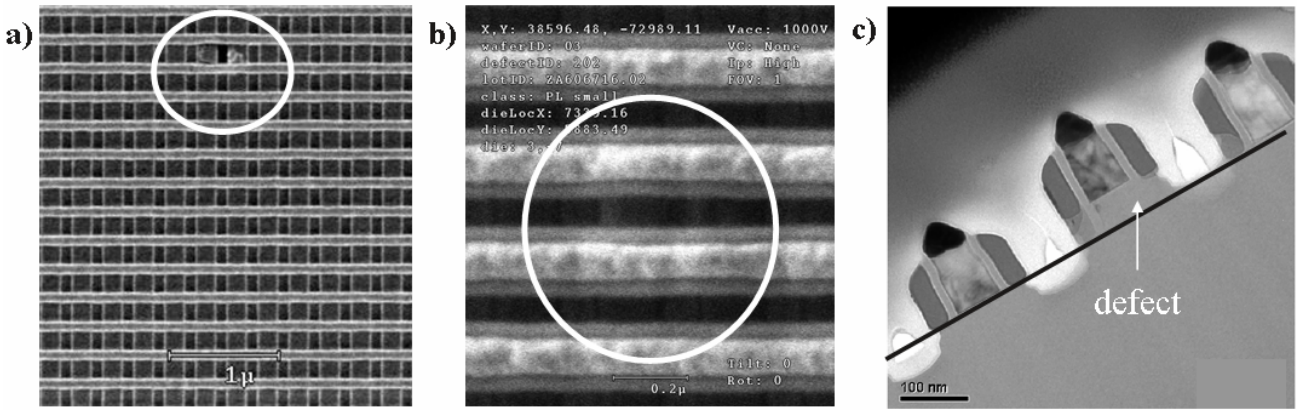

Fig. 3. a) Example of defect type of the 90 nm copper logic technology found by inline SEM review post poly gate main etch. b) SEM killer re-review post salicidation of the defect type of a). Only a faint shadow between the poly lines and a small protrusion of the poly lines themselves is visible. c) TEM failure analysis of defect type of a) and b) reveals root cause in isolation trench module. Wafer was processed until salicidation.

IV. Conclusion

Usually electrical fails require complicated cross-sectional or top-down failure analysis preparation techniques to find the root cause. In this work, we have presented a combination of data overlaying and selected SEM review of electrically failing structures, in order to rapidly provide a root cause for the fails and often save physical failure analysis capacities. The presented killer re-review can be performed as a standard review step in the process flow of the test chip or on engineering basis for excursion wafers, depending on which is more suitable for the yield status or the question to be solved. It was one important part of the efforts to improve the FEOL defect density related yield learning rate and to reduce FA costs during the 90 nm copper logic technology development.

Because of the short-flow processing, fast testing, the ability to test after salicide, and to re-review defects from all FEOL modules after the test on the wafers, the yield learning cycles were in days compared to weeks for traditional methods. The joint project of Infineon Technologies Dresden and PDF Solutions contributed to a doubling of the yield learning rate during the 90 nm copper logic technology development compared to the 130 nm logic technology development.

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