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Guide to Achieving World-Class Semiconductor Manufacturing Results

In manufacturing today's complex semiconductors, the old rules for achieving higher yields at mass production no longer apply.

Understanding the mechanisms of yield loss—and yield improvements—at 65nm and below requires a new understanding of yield. No longer driven by particulates and defectivity, yield is now more a function of balancing design content, manufacturing processes, and an effective production environment.

This guide describes how to consider yield at advanced manufacturing nodes and the methods and solutions available for increasing chip yield and profitability.

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Yield as a Strategic Imperative

High manufacturing yields are crucial to the success of electronic products and semiconductor manufacturers. This makes imperative the understanding of yield loss mechanisms for the rapid identification and mitigation of yield problems. Also fundamental for semiconductor manufacturers is predictability: of processes, production control, material management, resource allocation, and costs.

Yield models are a strategic tool for business and operations planning. Accurate yield models help create predictability and improve time to market and profitability. This is especially true with the increased production of complex ASICs, ASSPs, and SoCs, all of which are characterized by customized IP and options within a product.

Product Yields and the New Rules

Functional yield, characterized by stuck-at faults at test, is driven by defects and/or systematic issues. These defects are typically caused by particulates or other forms of gross contamination (which is assumed to be causing electrical failures) and are modeled as a number of defects per cm^2. Systematic issues were typically caused by aberrations in a process or design and managed through a set of rules and procedures.

However, with the move to process nodes below 90 nanometers (nm), the world changed. Conventional wisdom and rules about yield no longer apply. The contributions of particulate and defectivity to overall yield loss have decreased, but product yields have not shown a corresponding improvement. There are three major reasons that yield is now limited by design content features rather than by random defects:

1. The sheer number of features such as vias, contacts, lengths of metal wires, etc. has increased to the point where consistency of the order of single failures-per-billions (fpb) is required to achieve any yield. For example, vias are crucial features that limit overall yield, but their effects on yield cannot be realistically modeled by defects-per-area because of their relatively small open areas.
2. Tight tolerances associated with advanced technologies make old second-order issues into first-order problems. For example, plasma etch loading effects and corner rounding were always there, but were ignored as irrelevant second-order phenomena. With advanced processes, these mechanisms are killers, and require optical phase correction (OPC) and/or complex rule sets.
3. New materials and process technologies are precipitating a range of new systematic yield loss mechanisms. For example, in the move from aluminum to copper interconnects, newly required barrier materials such as tantalum nitride exhibit new failure mechanisms associated with via formation.
4. Small variations in the stability of the manufacturing process (tool-to-tool, chamber-to-chamber variability etc.) often lead to significant variability in resulting chip yields. Such manufacturing variations are difficult to detect (as their negative impact on yield

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can be dependent on design attributes of the specific product) and even more difficult to control.

Given these trends, it's clear that fundamental changes have occurred in the rules for managing functional yield:

- Cost and schedule constraints are such that engineering a yield solution through design iterations (requiring mask re-spins) is not an acceptable option for most products.
- The yield attributes of a given design must be quantified before the implementation of a design for yield. Managing the failure mechanisms requires accurate and comprehensive process characterization and design-process integration knowledge.
- A quantitative and credible yield prediction cannot be based on the traditional area-based yield model. Instead, it must be based on models related to the design content expressed in terms of the microscopic features that affect yield.

The iterative hand-off between process development and design groups does not work as it did in the past. Development of a set of design rules to describe the process capabilities, designing a product that is simply DRC-clean, and then relying on product re-spins to fine-tune a design or process is no longer adequate or realistic. New methodologies and techniques must be adopted.

New Techniques, New Rules

Semiconductor manufacturers need to trend toward a practice where a product is design based on an optimum product-specific set of trade-offs between performance, power, and cost (=yield) targets. A comprehensive, feature-based methodology can provide the optimum choice.

- *Begin with the Physics* - The various root cause failure mechanisms must be classified and understood, and the interactions between design attributes and process conditions cataloged.
- *Build a Model* – A catalog relating failure mechanisms to product failure modes (shorts, opens) must be defined based on a suitable classification of mechanisms, for example:
  - Line-shorts and opens, which are controlled by the interaction between the distribution of defect sizes and the corresponding line widths and/or spaces. These phenomena can be modeled using the critical-area concept.
  - Other mechanisms, such as hole-opens, are characterized by the failure rates of a given feature that corresponds to a given design layout and neighborhood, and that captures the relevant interactions with other process and design attributes.
  - Application-specific classifications to represent specific interactions with various design and process features. For example, models that describe antenna effects are affected by the ratio of the relevant areas and perimeters. Note that the models must be quite granular to be useful to a

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designer: the models must resolve the affect on yield of various layout features.

- *Characterize the Process* – Clearly, the process characterization must be based on suitable test chips to give visibility into the individual failure mechanisms and to provide observability into the failure statistics such that the various models can be calibrated for a given process technology. Doing this correctly is not trivial and must encompass these aspects:
  1. Defining the individual yield failure mechanisms and corresponding models.
  2. Defining the parameters to be measured so as to characterize the given yield mechanism.
  3. Defining and sizing the structures that allow the desired measurement so as to gain the desired statistical resolution.
  4. Defining and describing through a Design of Experiment (DOE) of test structures the dependence of the mechanism on various design variables.
  5. A complete set of test structures for all target process layers and for all design dependencies must be placed on a single test chip reticle, such that they can be individually accessed and tested.
  6. All individual structures must be tested on a statistically significant sample size, and the ensuing data reduced into a meaningful form for model calibration.
  7. Characterization data must capture the impact of process-variability (i.e. chamber-to-chamber deltas, tool-to-tool deltas and deltas across Preventive Maintenance cycles). Collecting such data effectively, efficiently, and accurately during mass production requires highly-compact scribe-line structures (non-intrusively embedded on product wafers) and fast-test (massive parallel testing) capabilities, as well as automated analysis.
- *Characterize the Design* – Design information for a given product must be extracted. Statistics for things such as critical areas, number of given features, characteristics of a given neighborhood effect—all are required. Additional multi-layer effects and information about connectivity or functionality may be required for some mechanisms.
- *Synthesize the Yield* – This bottom-up, content-based approach produces yield predictions that are more accurate than the phenomenologically defined top-down, area-based measures. However, this approach is far more complex than the simple die area and defect density-based models, and making it work requires methodologies that span multiple disciplines and have comprehensive technologies to make it all usable and accessible in practical terms.

New Perspectives in Yield Prediction

How does everything come together into a useful yield enhancement solution? Through a vertical “slice” of methodologies that spans specialized Characterization Vehicle test chips (including characterization of device

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variability and characterization of product wafers through the use of scribe characterization structures) plus yield modeling and design extraction enables an accurate yield simulation solution. Then it's possible to construct a matrix that presents yield loss contributions by individual process layers (or rows) and by individual, user-defined design blocks (or columns). Accumulation of the contributions, i.e., accumulation across all of the rows and columns, provides the overall product yield prediction.

This bottom-up yield synthesis really represents a paradigm shift in terms of how engineers relate to the yield predictions.

From the design perspective, the only useful information to be derived from traditional area-based yield models is that smaller is better. Consequently, designers could ensure that a design is manufacturable only by ensuring that the design successfully passes a Design Rule Check and is as small as possible.

With the bottom-up approach to manufacturability, and with yield information presented in a form that's sufficiently granular to resolve the correlation between the various design attributes and yield, the designer can understand and manage the manufacturability of the ICs. The degrees of freedom offered by this new approach encompass some of the following design activities:

1. *Design Planning*: an understanding of the yield contribution from various individual blocks (functions) allows the designer to architect a chip to meet the target cost parameters.
2. *Design Architecture*: the quantitative yield information available to a designer helps him or her make informed decisions at the architectural level. And, various redundancy schemes can be evaluated and selected to optimize product cost.
3. *Physical Design*: with granular yield information available to the designer, the layout (at both the IP and chip level) can be tuned to optimize product manufacturability and to select the best trade-off between all design attributes: performance, power, area, and yield.

Design for Manufacturing in Action

Yield simulation is just a foundational technology, as by itself, it produces no value. The real value is in *yield optimization*, achieved through process tuning and/or design tuning that's based on the quantitative information derived from the yield simulation 'foundation technology'.

The methodologies we described here are the basis of a comprehensive yield simulation technology developed by PDF Solutions. Over the last several years, this technology has been deployed and proven in numerous projects worldwide.

Design optimization is typically deployed in concert with process optimizations or as individual activities performed when the process is fixed and/or inaccessible. This optimization includes:

- *Layout optimization of standard cells and IP elements* – With quantitative and accurate yield prediction, the layout of pre-designed elements used in product designs is optimized to meet fixed performance, power, and/or area constraints, or may be traded off versus other design

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requirements. Elements that are yield-hardened can be swapped for standard elements; for existing designs; or for use in new designs for a true design-for-yield process.

- *Redundancy optimization of memories* – Use of the optimum redundancy amount and scheme—especially for designs that contain large memory blocks based on quantitative yield assessment of the overall die yield—is very important. The yield benefit associated with the use of redundancy can be very significant, especially during the process ramp phase when the process technology is not fully matured and memories are not yielding to their full potential.
- *Bit cell optimization of memories* – For small memory blocks, the use of redundancy is not appropriate. However, many small on-board memory blocks are not performance critical, and use of relaxed bit-cells can give significant yield improvement for die with multiple small memory blocks. The optimization again requires trade-offs between performance and yield and can be done only if quantitative yield information is available during the design phase.
- *Interconnect optimization:* Interconnect can be optimized and, if necessary, the yield characteristics can be traded with performance and/or density attributes. Use of wire-spreading and/or redundant vias has been well documented as an opportunity for yield hardening, and may have a significant effect on product yield. These approaches require trade-offs between multiple mechanisms contributing to yield loss. The optimum is defined based on quantitative yield simulation.

Manufacturability optimization of a given product may require one, some, or all of these activities. It depends on the design content, targeted process technology, and the costs and benefits associated with each of the changes.

Our experience with projects where the yield simulation technology has been used purely to optimize designs, i.e., without process optimization, shows typical net benefits of 10% to 15% improvement in yield, as averaged over the product lifecycle. When the technology is also used to optimize process, greater benefits are demonstrated.

Design for Yield and Manufacturability is an accepted practice. With the current moves to 65nm and 45nm, the nature of advanced process technologies, the complexity of SoCs, the costs of product development, and the pressures of the market, *the optimization of yield and manufacturability is clearly a strategic imperative.* Ignoring this fact is simply too risky.

To learn how PDF Solutions can help to improve the manufacturability and yield of your designs, contact the PDF Solutions office near you.
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