Predictive Yield Modeling of VLSIC's

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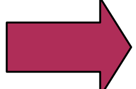
Outline



- Motivation, Objectives and Approach
- Defect Detection and Characterization
- Yield Impact Estimation
- Applications
- Conclusion

Motivation (1)

1.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00

Module: 0.61, 0.69, 0.77
DRAMDesign vs. Process: 0.98
Logic Design vs. Process: 0.67, 0.86
Speed: 0.92, 1.00
Other: 1.00
Overall Yield: 0.37, 0.59, 0.69

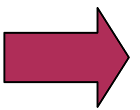
Target
Opportu
Present

Standby current

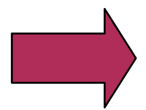
random metal defect and contact/ via failure reduction

systematic/random metal defect reduction

Systematic logic failures



Accurate quantification of yield issues allows comprehensive yield improvement planning



Predictive yield models provide one avenue for quantifying yield loss

Motivation (2)

100 chips manufactured

- 30 shipped to customer
  - 400 MHz parts 2 chips
  - 350 MHz parts 13 chips
  - 300 MHz parts 15 chips
- 70 rejected
  - Gross functional failures 44 chips
    - Systematic defect —12 chips
    - Unobservable systematic and random - 2 chips
    - **Random defect — 30 chips**
  - Unrepairable cache 14 chips
    - Systematic defect —0 chips
    - Unobservable systematic and random - 6 chip
    - **Random defect — 8 chips**
  - Speed <300 MHz 10 chips
    - 45% of t_clock is intrinsic RC interconnect delay
    - 55% of t_clock is dependent on active device performance and capacitance
  - All others 2 chips

Errors in quantification can lead to mis-estimation of systematic failure mechanisms

Motivation (3)

- **Yield loss mechanisms difficult to identify from sort data alone**
- **Empirical yield modeling methods insufficient for root cause identification**
  - not necessarily predictive (is today's solution valid tomorrow?)
- **Methods based purely on inline data do not account for design-related yield sensitivities**
- **Predictive defect limited yield modeling enables accurate separation and quantification of mechanisms**
  - can quantify by design block, defect type, process layer, etc.
  - each distinct electrical failure signatures modeled as a "micro-yield event"

Objectives

- **Determine target product yields**
  - Determine defect rates required to achieve product target yields
  - establish whether or not targets are realistic
- **Given a target or existing defect rate in the fab, determine the expected yield for a given product**
  - quantify systematic component of yield loss (yield gap analysis)
  - determine realistic product yield expectations
- **Quantification of yield loss contribution of each module or attribute**
  - rank problem modules or attributes
  - prioritize resources
  - determine yield gain expected if particular problem is fixed
- **Quantify lack of visibility of certain modules**
  - determine usefulness of developing new characterization vehicles

Summary of Approach

Inline Data

Electrical Test Chip Data

Memory bitmap Analysis

Defect detection and characterization

Product and Test Chip Layout Characterization

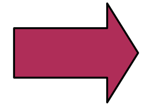
Yield Impact Table

Yield Improvement

Resource Allocation

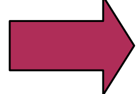
Product Planning

Yield Targeting



A modeling-based approach is a powerful tool for quantifying yield issues

Outline



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Methods for Defect Detection and Characterization

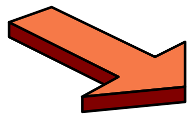
- Inline inspection
- Electrical Defect Characterization
- Memory Bitmap Analysis
- Binsort/Datalog Analysis

Inline Defect Inspection

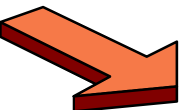
- **Inspection methods**
  - bright field (KLA 213x)
  - dark field (Surfscan 7xxx/AITx, Orbot WFxxx)
- **Review and classification**
  - SEM vs. optical review
  - ADC
- **Characterization**
  - Defect filtering
  - Size distribution analysis (only possible with bright field data)
  - Killer potential/Yield impact analysis

Inline Data Based DSD Model Fitting Task Flow

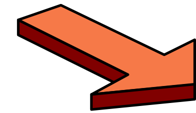
Raw KLA213X/KLA255x data



Filter by:
- Classification = shorts-related
- No cluster



Fit model for $x > x_f$



Evaluate model for $x > x_0$

- **Very important to filter/smooth data for compatibility with yield model**

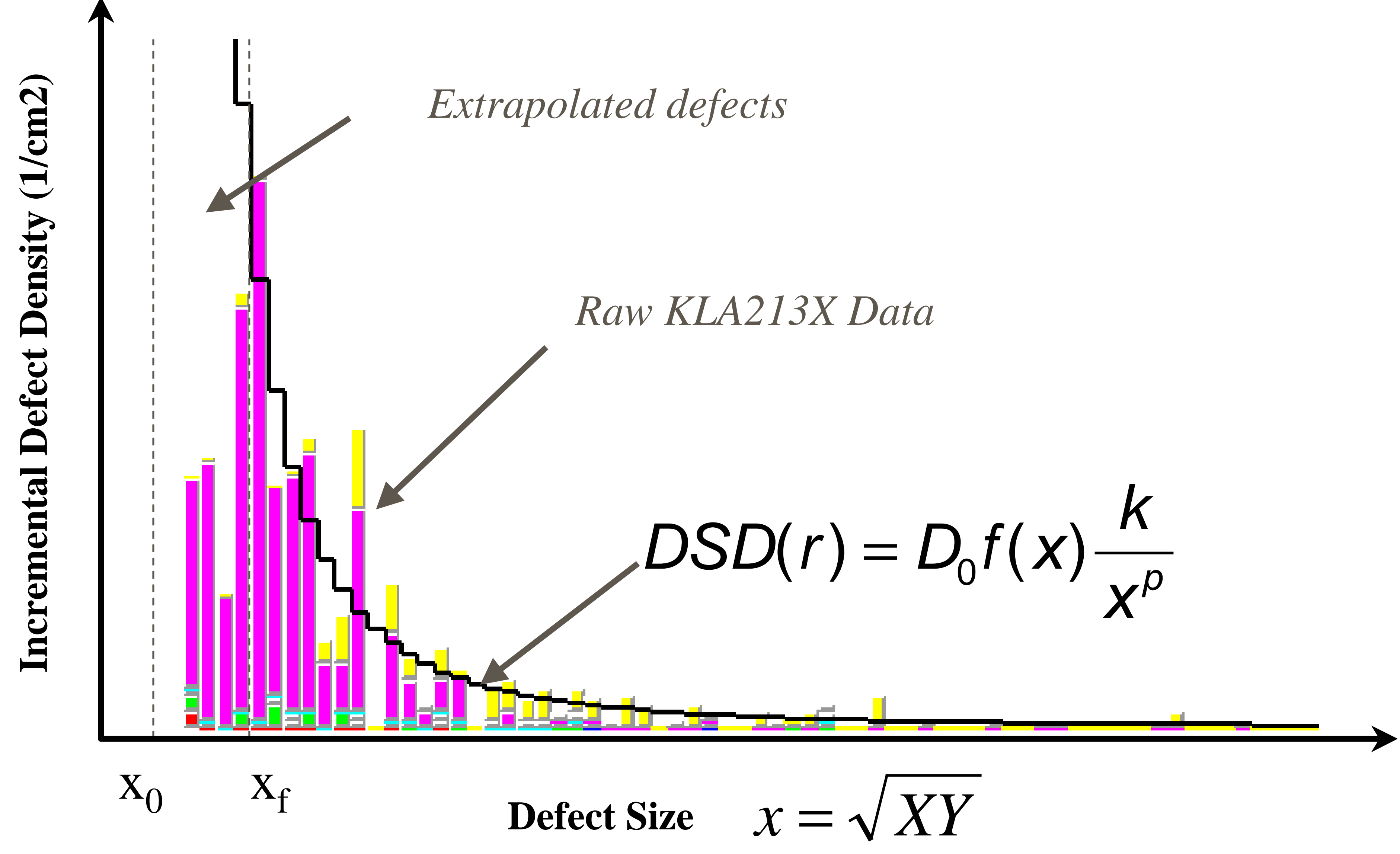
Defect Filtering

- **Include defect classifications related to shorts**
  - particles
  - planar shorts
  - any type of extra material

- **Discard other defect classifications**
  - missing material/open defect (build separate model)
  - missing via
  - corrosion
  - clusters (build separate model)
  - etc.

- **If partial review, must be careful to calibrate false defect rate using full review experiment**

Defect Size Distribution Modeling



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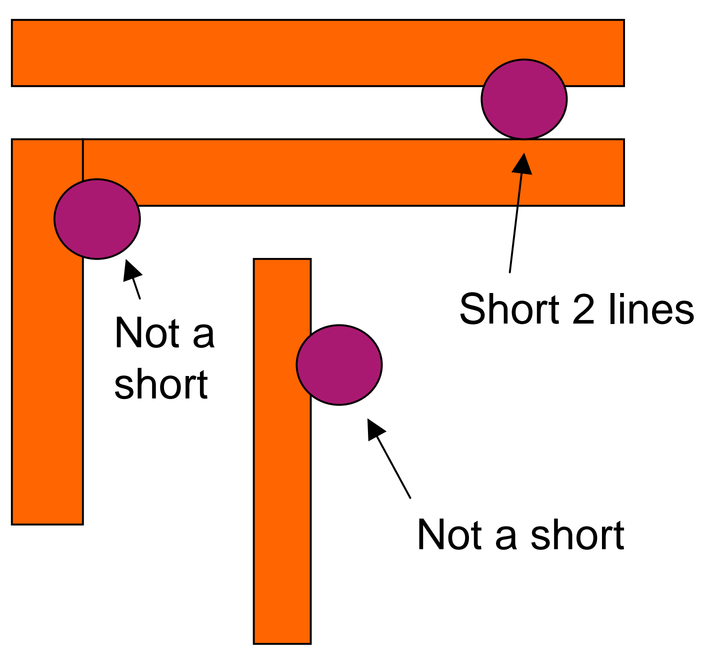
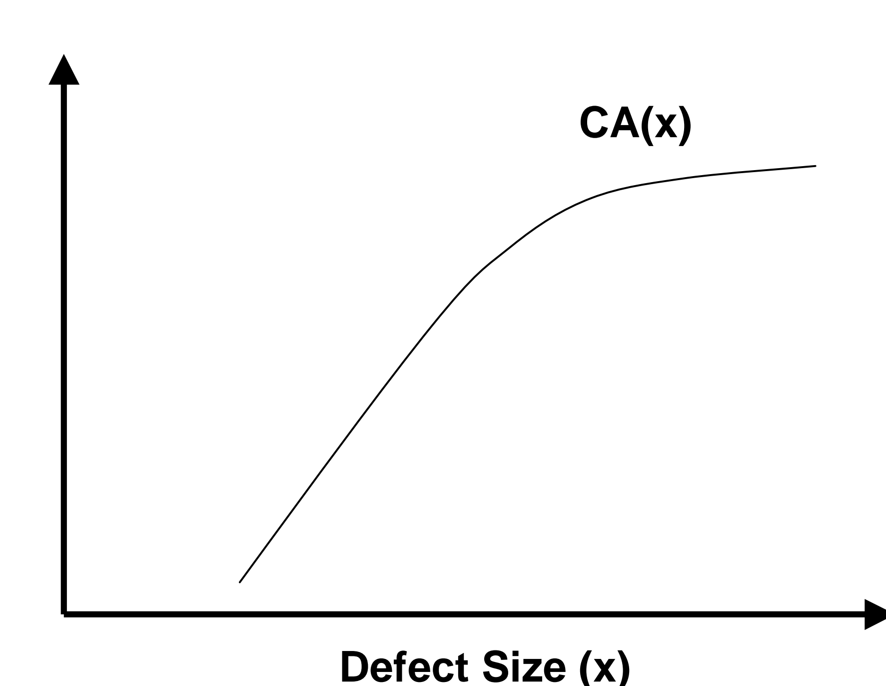
Critical Area Concepts

- **Critical Area, CA(x), is the area of the chip on which a defect of size x would cause a failure**

Example: Line Shorts



Example: Critical Area Curve for Shorts



Critical Area Concepts: Comb Example (2)

lw

ls

Defect of diameter *2ls+lw* causes at least 2 lines to short wherever it falls in the structure. CA(x) = Area of comb

Area

L*(ls+lw)n = Area of Comb

X

2ls+lw

Defect Diameter

lw

ls

Defect of diameter *> 2ls+lw* causes at least 2 lines to short wherever it falls in the structure. CA(x) = Area of comb

Note the linear trend in CA(x) due to regular comb structure.

Area

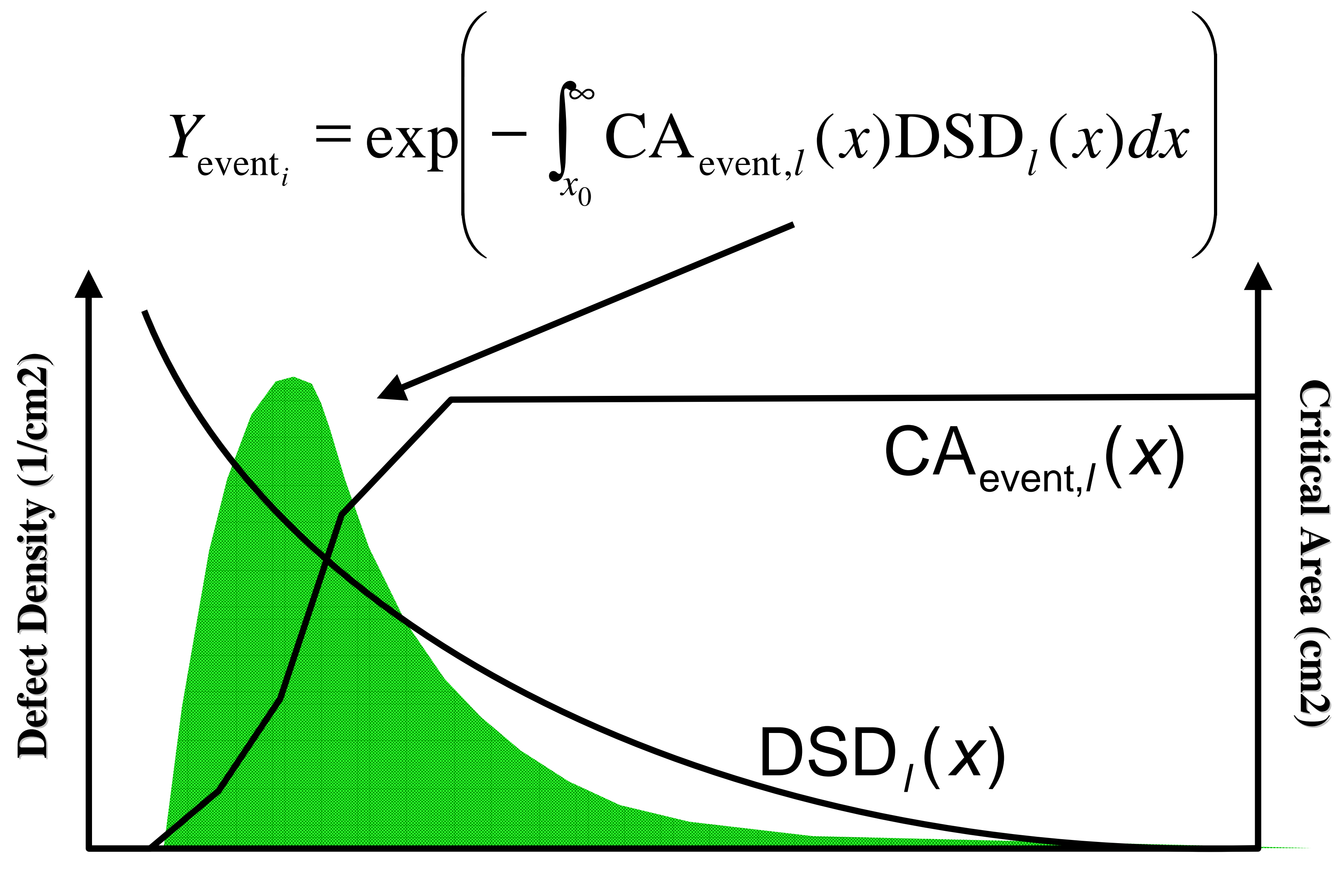
CA(x)

X

2ls+lw

Defect Diameter

Yield Event Prediction



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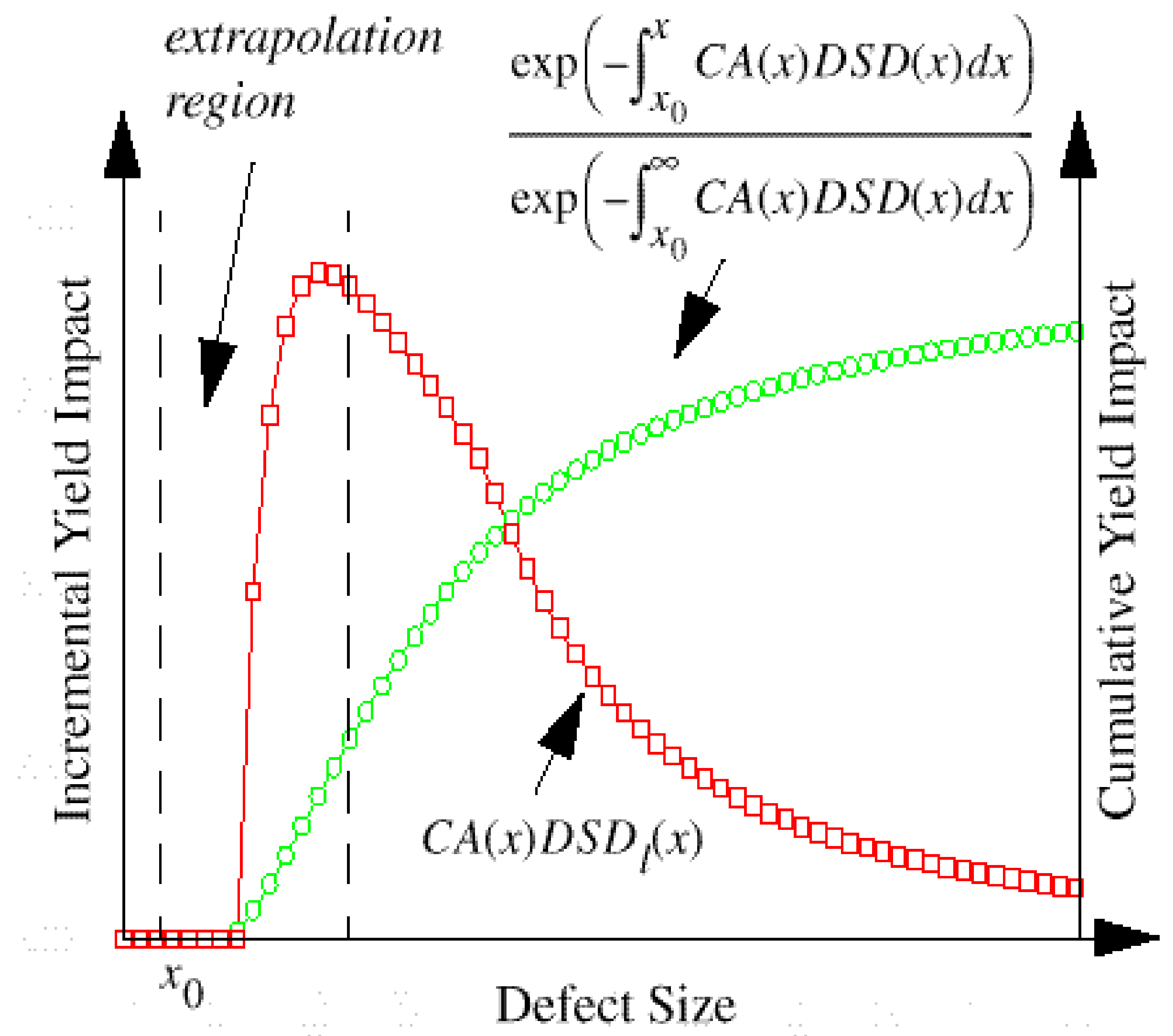
Yield Impact vs. Defect Size



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- **Defect Detection and Characterization**
  - Inline Inspection
  - Electrical Detection
  - Memory Bitmap Analysis
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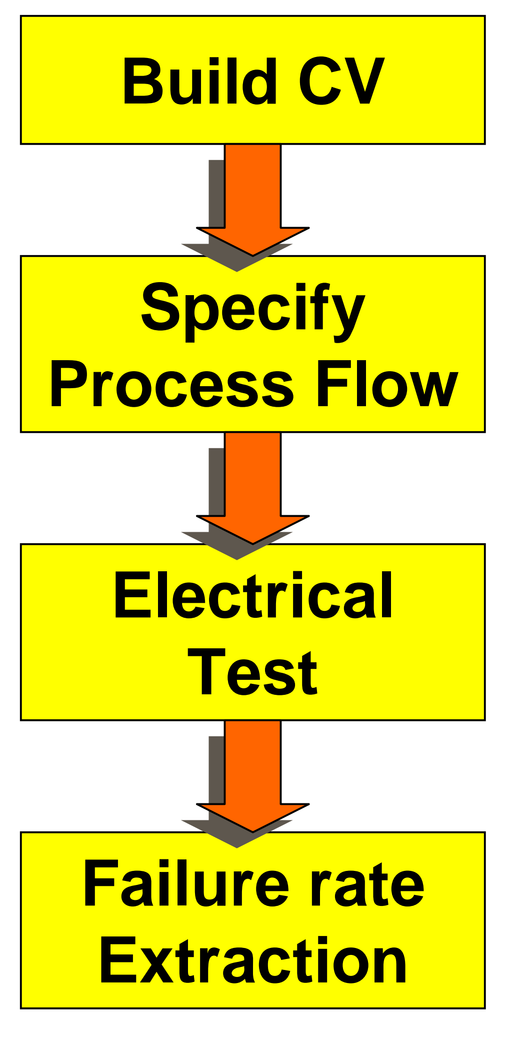
Electrical Defect Detection and Characterization



- Mimic product patterns and pattern distributions
- Keep wafer state consistent with full flow
- Consider test time during design phase
- D0, p, Df, lambda

Typical Metal/Poly Planar Layer Short Flow CV

POLYSF_TOP

~22mm

Linewidth characterization

Systematic open/short yield characterization

Random defect characterization

Nest Test Structure for DSD Extraction

S

N_snakes

LW

Same total critical area as large comb, but possible to calculate size of defect

Nest Test Structure - Concept

n: no. of lines

2-line shorts

n: no. of lines

3-line shorts

n: no. of lines

N-line shorts

Number of Lines Shorted	Count
2	29
3	10
4	4
5	0
6	1

Nest Test Structure - Ideal Critical Area

3-line shorts

2-line shorts

4-line shorts

>4-lines shorted

Critical Area

Defect Size

Nest Test Structure - Actual Critical Area

Critical area (um^2)

3000000
2500000
2000000
1500000
1000000
500000
0

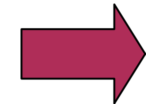
0 1 2 3 4 5 6 7 8

Defect Radius (um)

Ideal curves

Actual curves lose 1/16th of total area due to snake signal aliasing

2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
Grand Total
ideal 2



Practical implementation of NEST idea requires advanced layout analysis for accurate defect size characterization

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Nest DSD Model Fitting Task Flow

Raw E-Test data

Filter data by wafer position and design rule of structure

Derive failures from parametric values

Nest structure Critical Area

Fit D0,p parameters

Metal Defect Size Distribution Example Results

Do = 1.69 , p = 2.23

Observed Lambda
Predicted Lambda

Lambda

0.0
0.005
0.010
0.015

below DR at DR above DR1 above DR2 above DR3

Using multiple nests below, above and at design rule can expose process marginalities

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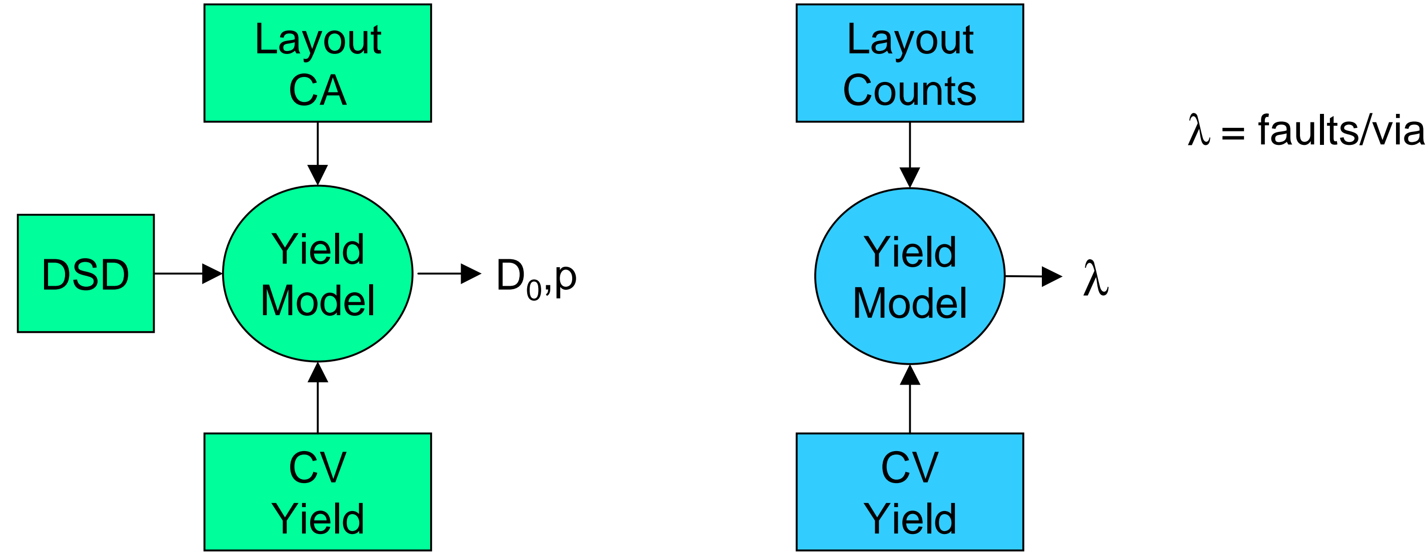
Contact, Via Hole Opens Yield Modeling

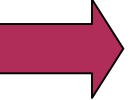
- **Likelihood of a particle defect causing hole open is low**
- **Hole opens typically caused by randomly occurring systematic issues**
- **Estimate hole fault rate directly from test structures such as chains**



Example Via Short Flow CV

Via Chains

Metal vs. Via checks



Via chain and single-via kelvin test structures are constructed in various configurations which mimic product layout attributes

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Hole Open Fail Rate Model Fitting Task Flow

Raw E-Test data

Filter data by wafer position and design rule of structure

Derive failures from parametric values

Number of holes in Via Chain

Fit λ parameter

Example Via CV Results

SubDOE = WithN

log Rc

-0.065 -0.04 -0.02 0 0.02 0.04 0.065

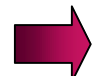
ViaAndUpperLayerMisalignmentVersusLowerLayer

SubDOE = WithoutN

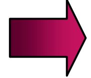
log Rc

-0.065 -0.04 -0.02 0 0.02 0.04 0.065

ViaAndUpperLayerMisalignmentVersusLowerLayer



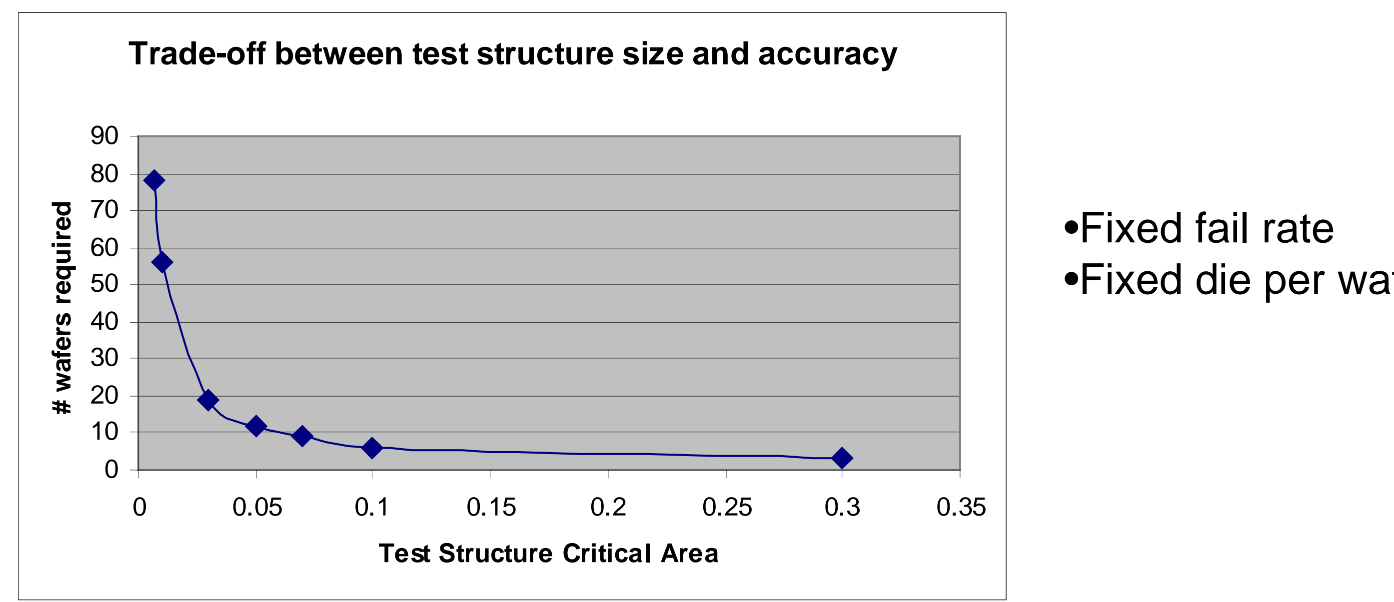
Via resistance/yield dependent on metal neighborhood



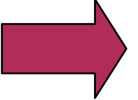
Can use lambda vs. misalign for yield prediction

Electrical Defect Detection Sampling Considerations

- A trade-off exists between the test structure size and the accuracy of the fail rate calculations.
- As the test structure size decreases, more wafers are required to calculate the fail rate calculations with statistical confidence



•Fixed fail rate
•Fixed die per wafer



Must use sufficient sampling size when calculating the failure rates

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Memory Bitmap Analysis

Goals

- Map Failed Bit Map Codes (Failure Modes) to the most likely defect mechanisms
- Failure Modes defined as *Yield Micro-events* in our Yield Impact Evaluation
- Pareto of defect mechanisms (per layer and defect type) evaluated using critical area and DSD
- separation of defects into two groups: in the memory array and outside of array (sense amp, decoders, datalines)

Applications

- root cause analysis
- aid to analytical Failure Analysis (deprocessing, FIB SEM)
- hit rate estimate for in-line detected defects

Defect Detection and Characterization Summary

Method	Pros	Cons
Inline inspection	Leverages product wafers already in fab Excellent defect localization	Throughput/TAT Sensitivity can be poor Killer potential not always clear Systematic failures not always observable
Electrical CV	Good observability systematic defects Good observability random defects Killer potential often obvious Turnaround time	Requires engineering wafers Fault localization can be difficult Root cause not clear
Memory Bitmap	Excellent fault localization Good root cause identification Killer potential is obvious	Throughput/TAT Poor observability of random logic faults Requires full flow processing
Datalog Binmap	Killer potential is obvious Captures all failure modes	Fault localization poor Root cause usually not clear Requires full flow processing Huge cost

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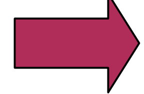

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Building The Overall Yield Impact Prediction

Product

block A | block B | block C

Process

Process step	Failure mode
AA	short
Poly	short/open
Contact	open
Metal1	short
Via	open
Metal2	short

Yield Impact Table

The PDF Yield Impact Table

- **Example table for 2 level metal logic chip with embedded SRAM:**

Yield of poly layer in SRAM

	poly	contact	metal1	via	metal2	Total across chip layers
Logic	Y_Logic,poly	Y_Logic,contact	Y_Logic,metal1	Y_Logic,via	Y_Logic,metal2	Y_Logic
SRAM	Y_SRAM,poly	Y_SRAM,contact	Y_SRAM,metal1	Y_SRAM,via	Y_SRAM,metal2	Y_SRAM
Total across chip blocks	Y_poly	Y_contact	Y_metal1	Y_via	Y_metal2	Y_chip

Yield of layer computed by taking product down column of all block yields

Yield of poly layer computed by taking product down column of all block yields

Redundant Yield Modeling

- Repaired yield prediction is easily handled by yield impact table paradigm
- Critical areas for each micro-event are treated as separate “blocks” in layout
- Each event receives a separate column or row in yield impact matrix
- If event can be repaired, cell in yield impact table treated as 100%yield

Example Micro-event Critical Areas

VDD

i0

i1

bit

bitbar

word

GND

Event Categorization

Event Categorization
Vdd,i0 bitbar,i1 word,GND i0,bit
i1,i0
bit,word i1,word
i0,bit,word i1,bitbar,word Vdd,i0,i1
Vdd,i1 i0,word bitbar,word

- **Micro-event critical areas are disjoint**

Example Micro-event Critical Area Curves

Normalized Critical Area

1.0 0.5 0.0

Event1

Event2

Layer1

1.0 0.5 0.0

Layer2

Defect Size

Redundant Yield Model Formulation

Yield Impact Prediction

memory block

Logic block A

Logic block B

2 column short

3 column short

>3 column short

2 rows short

other event short s

missing cell contact

Repairable Events

Unrepairable Events

repaired yield impact prediction

virgin yield impact prediction

Micro-event Yield Impact Matrix

- **Event Yields:**

LAYER/EVENT	1bit	2bit	nword	2word	blk1	blk2	nbl	2bl	nbita	nbitb	cross	other	TOTAL
Poly1	96.8%	99.8%	99.8%	99.4%							98.7%	98.7%	93.4%
Poly2	88.0%	99.3%			95.7%	96.9%	99.3%	99.3%				99.3%	79.5%
Poly3		61.2%							95.8%	92.6%		98.5%	53.5%
Metal			95.8%	93.0%									89.1%
Virgin Core	85.2%	60.7%	95.6%	92.4%	95.7%	96.9%	99.3%	99.3%	95.8%	92.6%	98.7%	96.6%	35.4%
C-BL		7.1%											7.1%
C-BIT	39.1%												39.1%
Virgin Core	33.3%	4.3%	95.6%	92.4%	95.7%	96.9%	99.3%	99.3%	95.8%	92.6%	98.7%	96.6%	1.0%
Repaired Core	repaired	repaired	95.6%	repoair	repaire	repaire	99.3%	repaire	repaire	repaire	98.7%	96.6%	90.6%

- **Event Fail Frequency (1-Yield):**

LAYER/EVENT	1bit	2bit	nword	2word	blk1	blk2	nbl	2bl	nbita	nbitb	cross	other	TOTAL
Poly1	3.2%	0.2%	0.2%	0.6%							1.3%	1.3%	6.6%
Poly2	12.0%	0.7%			4.3%	3.1%	0.7%	0.7%				0.7%	20.5%
Poly3		38.8%							4.2%	7.4%		1.5%	46.5%
Metal			4.2%	7.0%									10.9%
Virgin Core	14.8%	39.3%	4.4%	7.6%	4.3%	3.1%	0.7%	0.7%	4.2%	7.4%	1.3%	3.4%	64.6%
C-BL		92.9%											92.9%
C-BIT	60.9%												60.9%
Virgin Core	66.7%	95.7%	4.4%	7.6%	4.3%	3.1%	0.7%	0.7%	4.2%	7.4%	1.3%	3.4%	99.0%
Repaired Core	repair	repair	4.4%	repair	repair	repair	0.7%	repair	repair	repair	1.3%	3.4%	9.4%

Yield Model Forms and Definitions

- **If defects occur uniformly across wafer/die, can use simple Poisson Model:**

  $Y = e^{-\text{faults/chip}}$ in general

  $Y = e^{-Do^*Ac(p)}$ for critical area-based defects (poly, metal layers)

  $Y = e^{-\lambda * N}$ for counted defects (contacts, vias)

  where

  D_0 = defects/cm^{2}; $Ac(p) = \int_{x_0}^{\infty} CA(x) \frac{k}{x^p} dx$

  λ = fails/count; N = # of counts

- **If defect distribution is not uniform, should use other yield models**
  - Modified Poisson, Negative Binomial, Murphy, Bose-Einstein, Seeds

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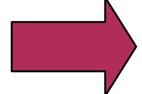

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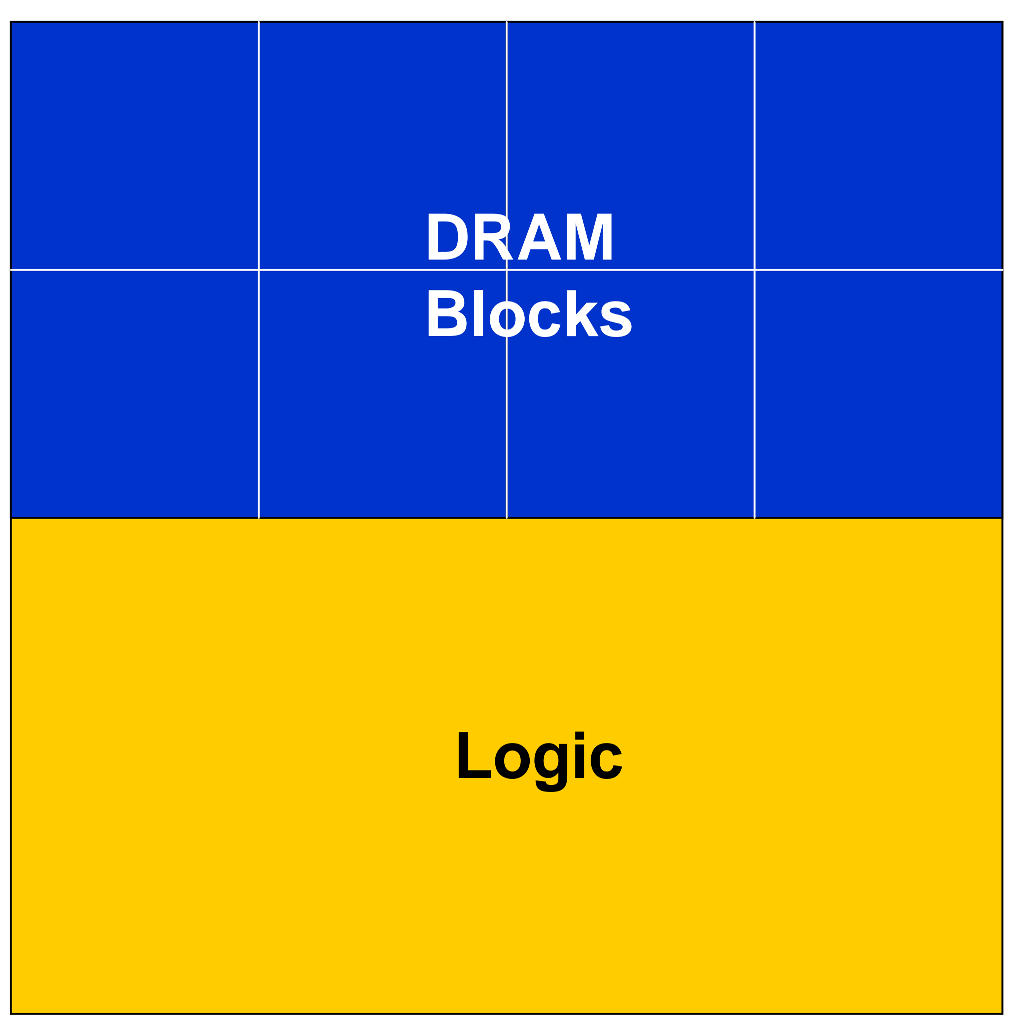
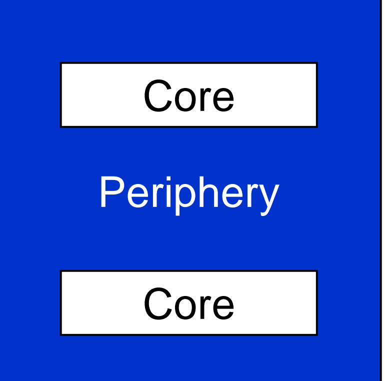
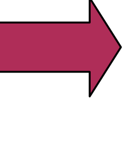
Applications of Predictive Yield Models

- **Yield impact estimation for Embedded DRAM chip**
- **Yield gap analysis for high performance logic with embedded memory**
- **Yield prediction for FLASH memory redundancy performance**
  - ASMC 1998

Yield Impact Estimation for Embedded DRAM Chip







The logic and DRAM blocks, and the core and periphery within DRAM blocks are treated separately in yield impact table

Yield Impact Table for eDRAM Chip

Layers / Blocks	Unrepaired Core	Repaired Core	Unrepaired Periphery	Repaired Periphery	DRAM Unrepaired Virgin	DRAM Repaired	LOGIC	Total Virgin Chip Yield	Total Repaired Chip Yield
Poly1	88.58%	99.53%	94.46%	97.30%	83.67%	96.84%	92.25%	77.19%	**89.34%**
Poly2	77.60%	98.89%	100.00%	100.00%	[illegible]	[illegible]	[illegible]	77.60%	**98.89%**
Poly3	[illegible]	99.47%	100.00%	100.00%	[illegible]	[illegible]	[illegible]	81.36%	**99.47%**
Metal1	[illegible]	100.00%	[illegible]	93.05%	89.04%	93.05%	82.18%	73.18%	**76.47%**
Metal2	[illegible]	100.00%	[illegible]	85.56%	85.56%	85.56%	89.43%	76.52%	**76.52%**
Metal3	[illegible]	100.00%	[illegible]	94.46%	94.46%	94.46%	85.86%	81.10%	**81.10%**
Metal4	[illegible]	[illegible]	[illegible]	[illegible]	97.39%	97.39%	95.65%	93.15%	**93.15%**
Metal5	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	100.00%	99.02%	99.02%	**99.02%**
Shorts Total	**55.93%**	**97.90%**	**66.21%**	**71.27%**	**37.03%**	**69.77%**	**55.13%**	**20.41%**	**38.47%**
C-N+AA	100.00%	100.00%	97.90%	97.90%	97.90%	97.90%	94.01%	92.03%	**92.03%**
C-P+AA	100.00%	100.00%	98.80%	98.80%	98.80%	98.80%	93.59%	92.46%	**92.46%**
C-POLY	100.00%	100.00%	96.57%	96.57%	96.57%	96.57%	95.92%	92.63%	**92.63%**
Via12	100.00%	100.00%	98.68%	98.68%	[illegible]	[illegible]	95.38%	94.12%	**94.12%**
Via23	[illegible]	[illegible]	[illegible]	99.80%	[illegible]	[illegible]	98.19%	97.99%	**97.99%**
Via34	[illegible]	[illegible]	[illegible]	99.94%	[illegible]	[illegible]	99.32%	99.26%	**99.26%**
Via45	100.00%	100.00%	[illegible]	99.98%	99.98%	[illegible]	100.00%	99.98%	**99.98%**
C-BL	38.29%	100.00%	[illegible]	100.00%	38.29%	[illegible]	100.00%	38.29%	**100.00%**
C-WL	61.88%	100.00%	100.00%	[illegible]	61.88%	[illegible]	100.00%	61.88%	**100.00%**
C-BIT	61.88%	100.00%	100.00%	[illegible]	61.88%	[illegible]	100.00%	61.88%	**100.00%**
Opens Total	**14.66%**	**100.00%**	**91.91%**	**91.91%**	[illegible]	**91.91%**	**78.49%**	**10.58%**	**72.14%**
Total	**8.20%**	**97.90%**	**60.85%**	**65.50%**	**4.99%**	**64.12%**	**43.28%**	**2.16%**	**27.75%**

Big Sensitivity to Metal1

Low unrepaired yield...

...but most defects repairable

Overall Yield strong Function of Metal1 and Via12 Logic Yield

Predicted Repaired DRAM Yield better than Logic Yield Block

Yield Impact Table for eDRAM Chip (cont'd)

Predicted Yields can further be broken down into individual logic blocks yields...

No apparent block-specific M1 problem because all logic blocks are equally sensitive to M1.

Layers/ Contacts	D0	BlockA	Block B	Block C	Block D	Block E	Block F	Block G	Block H	Block I	Block J	Block K	Other	Total Yield
Polly1	**D0_P1**	99.9%	99.9%	99.9%	100.0%	100.0%	99.9%	99.9%	100.0%	100.0%	100.0%	100.0%	98.0%	**97%**
Metal1	**D0_M1**	99.5%	99.9%	99.9%	100.0%	99.9%	99.8%	99.9%	99.8%	100.0%	99.9%	99.9%	99.6%	**98%**
Metal2	**D0_M2**	99.8%	99.9%	99.9%	100.0%	100.0%	99.9%	99.9%	99.9%	100.0%	100.0%	100.0%	99.9%	**99%**
Metal3	**D0_M3**	99.5%	99.9%	99.9%	100.0%	99.9%	99.9%	99.9%	99.9%	100.0%	100.0%	99.9%	99.7%	**99%**
Metal4	**D0_M4**	99.8%	99.7%	99.9%	100.0%	99.9%	99.8%	99.8%	98.8%	100.0%	100.0%	99.9%	100.0%	**98%**
Shorts Total	**λ (fails/1e9)**	**99%**	**99%**	**100%**	**100%**	**100%**	**99%**	**100%**	**98%**	**100%**	**100%**	**100%**	**97%**	**91%**
C-N+AA	**λ_N+AA**	94.9%	96.6%	97.9%	99.1%	98.7%	97.1%	98.0%	97.9%	99.3%	99.4%	97.9%	99.2%	**78%**
C-P+AA	**λ_P+AA**	93.5%	97.5%	97.1%	98.8%	98.3%	96.3%	97.3%	97.4%	99.0%	99.2%	97.3%	98.7%	**74%**
C-Poly1	**λ_Poly**	95.8%	96.9%	98.4%	99.4%	99.2%	97.8%	98.4%	98.6%	99.1%	98.9%	98.5%	99.0%	**82%**
Via12	**λ_v12**	99.7%	99.8%	99.9%	100.0%	99.9%	99.9%	99.9%	99.9%	99.9%	99.9%	99.9%	100.0%	**99%**
Via23	**λ_v23**	99.9%	99.9%	100.0%	100.0%	100.0%	99.9%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	**100%**
Via34	**λ_v34**	[illegible]	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	**100%**
Opens+ Shorts Total		[illegible]	**91%**	**93%**	**97%**	**96%**	**91%**	**94%**	**94%**	**97%**	**97%**	**94%**	**97%**	**47%**
Total		[illegible]	**90%**	**93%**	**97%**	**96%**	**91%**	**93%**	**92%**	**97%**	**97%**	**93%**	**94%**	**42%**

Block A is most sensitive to Contact Failures

Conclusions From eDRAM Yield Prediction

- Logic yield loss more significant than DRAM yield loss, after accounting for repair
- Metal1 significantly affects all logic blocks
- Logic block A is sensitive to Contact yield and may benefit from re-design with redundant contacts

Yield Gap Analysis

Electrical CV Data

Nominal D0, p and λ

D0, p and λ Variation

Product Design

Layout

Wafer Sort Test Data

Yield Prediction: Nominal, 3σ

Compare

Actual Yield: Nominal, 3σ

Yield Gap Analysis Result

Yield

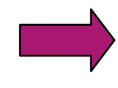
100%
80%
60%
40%
20%
0%

Mean value variation in DRAM and Logic yields due to METAL and CONTACT module defects

0% mean shift

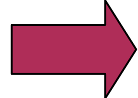
Systematic logic yield gap with parametric signature

Virgin Memory (Predicted)
Virgin Memory (Observed)
Repaired Memory (Predicted)
Repaired Memory (Observed)
Logic (Predicted)
Logic (Observed)



Metal module defects, contact module defects and logic yield gap were target areas of diagnosis work

Outline

- Motivation, Objectives and Approach
- Defect Detection and Characterization
- Yield Impact Estimation
- Applications

- Conclusion

Conclusions

- **Determine target product yields**
  - Determine defect rates required to achieve product target yields
  - establish whether or not targets are realistic
- **Given a target or existing defect rate in the fab, determine the expected yield for a given product**
  - quantify systematic component of yield loss (yield gap analysis)
  - determine realistic product yield expectations
- **Quantification of yield loss contribution of each module or attribute**
  - rank problem modules or attributes
  - prioritize resources
  - determine yield gain expected if particular problem is fixed
- **Quantify lack of visibility of certain modules**
  - determine usefulness of developing new characterization vehicles

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