ROBUST MESH GENERATION FOR FAST, ACCURATE AND STABLE TCAD

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Abstract

This paper describes a solution to a problem universally recognized as a potential show-stopper in TCAD: robust triangulation of complex device structures in particular at the interface between multi-dimensional process and device simulation. Triangulation in TCAD is critical for several reasons: computational efficiency and robustness favor well-shaped elements and small node counts, accuracy dictates placing dense uniform layers of elements at junctions and inversion layers. The accuracy requirements become particularly important for statistical TCAD applications, where gridding noise can overpower useful information. To keep such noise low, special care must be exercised in the gridding process.

The conventional approach to multi-dimensional integrated TCAD is to use the same triangulation for both process and device simulations. The needs of the device simulation thus are incorporated into the mesh utilized during the process simulation. This mesh is a "compromise" one, which is typically very large and frequently of poor quality. As a result, mesh sizes on the order of 3000-7000 nodes for a submicron MOSFET and even larger for complex power devices are common, leading to very long simulation times and in some cases convergence problems (particularly with large isolation structures and power devices). Statistical applications of TCAD where a large number of simulations are required to sample the design space further aggravate this problem.

A novel strategy to generate such grids is described and application examples are presented in this work. The proposed meshing algorithm preserves the complexity of the original structure while allowing precise placement of mesh nodes and lines at the locations required for accurate device simulation. The remeshing procedure decouples the process simulation mesh from the device simulation mesh. As a result, both can be made much smaller without loss of accuracy allowing a dramatic speed-up of the overall simulation (typically 5-25X).

The New Meshing Algorithm

The proposed algorithm has been implemented in a tool called pdMesh [1],[2] available from PDF Solutions, Inc. The fundamental strategy of the proposed method is to place mesh nodes and element edges in the simulation domain according to the application-specific needs of the problem and then connect them to a Delaunay mesh using a robust triangulation engine [3]. The main characteristics of the approach are as follows:

- Using a powerful extension language (Tcl) to adapt to particular device types and specific requirements to the mesh to be generated. Layers of mesh nodes can be placed explicitly where they are needed.
- Original material boundaries as generated by the process simulator are preserved. Only modifications to boundaries as requested by the user in the Tcl control file (device-type specific meshing template) are performed. These can include refining and unrefining the boundary. Complex geometries do not pose a stability problem as commonly observed with quad-tree based algorithms.

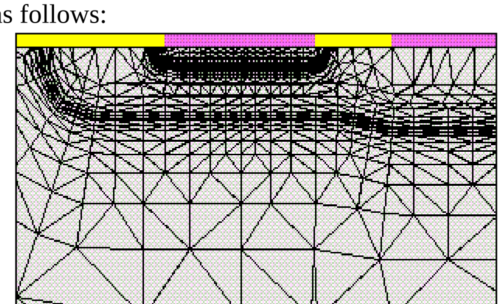


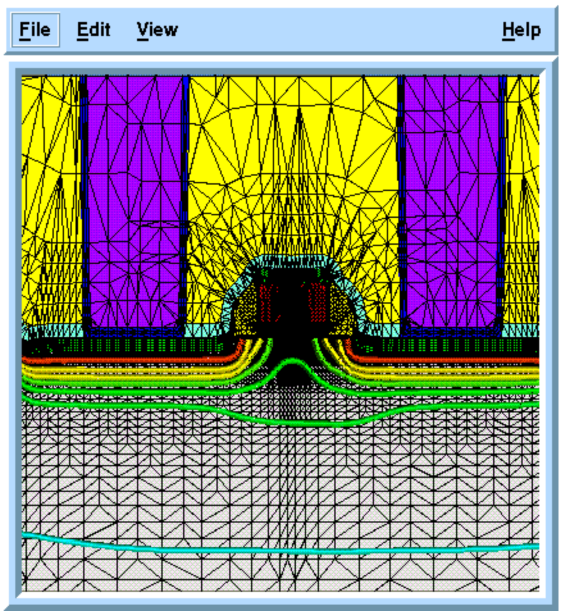
Figure 1 A BJT mesh created with pdMesh

- Layers of mesh nodes can be placed along material interfaces (for MOS channels) and along any contour of an analytic expression (e.g. a pn-junction, a certain doping value, equipotential line, etc.) This allows the user to adapt the mesh to both the particular geometry and a previously obtained process or device simulation result.
- Highly anisotropic meshes can be created, which are essential to treat inversion layers, pn-junctions, etc. As examples Figure 1 shows a BJT mesh and Figure 3 shows a MOSFET mesh.

Application Example

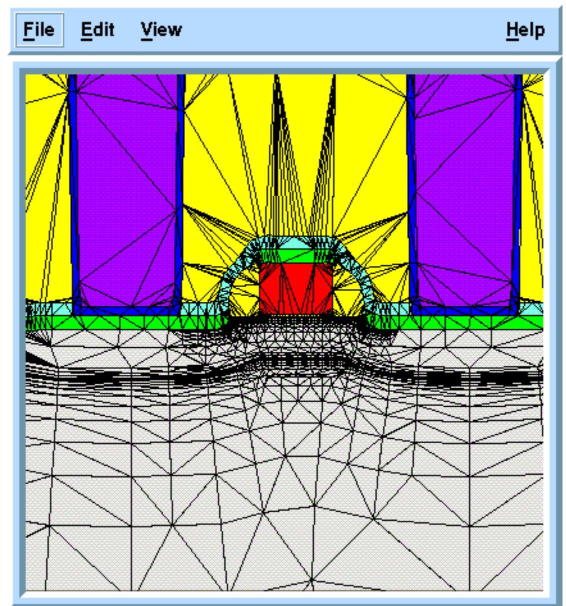
An industrial application is used to demonstrate the new algorithm in a realistic setting. The device is a 0.35 micron

PMOS developed by a major US semiconductor manufacturer. The process was simulated with TSUPREM-4 [4] using a “compromise” initial mesh designed to provide sufficient resolution for the subsequent device simulation. The resulting mesh has 7600 nodes and is shown in Figure 2. A new mesh generated by pdMesh is shown in Figure 3. As seen in Figure 3 mesh layers were placed in the channel as well as in the junctions of the device. A vertical channel mesh resolution of 2nm is achieved despite an overall low node count of 1400. This channel mesh spacing was chosen to match the channel resolution of the reference TSUPREM-4 mesh (Figure 2). To validate the quality of the new mesh in comparison to the original one, a gate curve (Id vs. Vg) was generated using both structures and showed less than 0.1% difference in Vth (see text below Figure 2, Figure 3). The two gate curves are almost identical as shown in Figure 4. A comparison of CPU times as shown below the Figures indicates a speed-up of about 20X.



Vth=-1.171V, 30 min (UltraSparc1, Id vs. Vg)

Figure 2 Original TSUPREM-4 structure and mesh



Vth=-1.172V, 1.3 min (UltraSparc1, Id vs. Vg)

Figure 3 New mesh generated by pdMesh

Conclusions

The new meshing procedure was shown to dramatically improve TCAD simulation speed and accuracy by decoupling the device simulation mesh from the one used in process simulation. The algorithms creates highly anisotropic mesh layers which resolve channels, pn-junctions, etc. The resulting mesh respects the original geometry and is adapted to the physics of the device under consideration.

References

[1] PDF Solutions, “*pdMesh User’s Manual*”, 1997
[2] V. Axelrad, “*Robust and Accurate Mesh Generation for Statistical TCAD Applications*”, PDF Solutions, White Paper, Dec. 1996
[3] J.R. Shewchuk, “*Triangle: Engineering a 2D Quality Mesh Generator and Delaunay Triangulator*”, First Workshop on Applied Computational Geometry (Philadelphia, Pennsylvania), pages 124-133, ACM, May 1996
[4] Technology Modeling Associates, “TSUPREM-4”, 1996

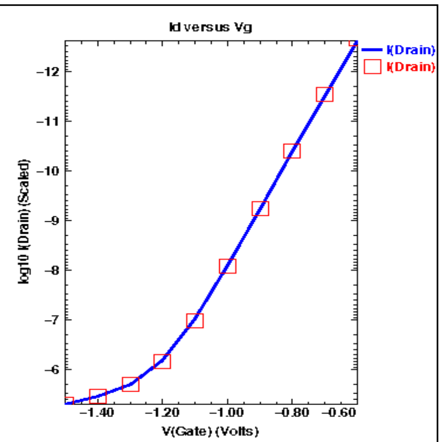


Figure 4 Id versus Vg data generated with both meshes: squares using the original mesh, solid line using the new pdMesh-generated one.