Yield Improvement
Using a Fast Product Wafer Level Monitoring System

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Abstract – A Scribe Characterization Vehicle®, (CV®) Test Chip has been developed to enable a fast turn around mass production yield monitoring system. The test chip design is being placed within the scribe lines of product chip reticles, efficiently utilizing three-dimensional stacking of test structures. During manufacturing, wafer level testing will be executed using pdFasTest® to ensure test times below 10 minutes per 300mm wafer. The measurement data will then be analyzed using pdCV™ to determine yield predictive data like fail rates and defect densities. Also variability data of layer specific parameters like sheet resistance and contact/via resistance will be extracted. Finally, extensive statistical analysis will be run using *data*POWER™ to derive correlation to product yield as well as lot equipment history.

1 Introduction

Putting smart monitors into the scribe line area is becoming more popular in sub100nm technologies due to an increased number of potential manufacturing problems, which cannot be efficiently evaluated by just using simple passive test structures. [DDGY05] reports the usage of SRAM and ROM based small test cells to identify BEOL related issues. As typical for memory based designs, its emphasis is on failure localization. For testing an expensive memory tester is required, which usually is not available at a manufacturing site. Furthermore, testing is too slow for monitoring each test chip on every wafer during mass production.

We are introducing a more comprehensive and robust wafer level yield monitoring system, which enables fast turn around data analysis. Section 2 will describe the design concept of the Scribe CV test chip that is used to collect mass production data. Section 3 will introduce pdFasTest which ensures fast wafer level testing. Finally, experimental results will be discussed in Section 4.

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2 Scribe CV Design

Generally, simple test structures are used to extract yield relevant parameters [Bueh83], [DGGY05]. For instance, chains of contacts and vias are used to monitor fail rates of contact and via layers. Snake and comb type test structures are used to extract single layer defect densities. Those structures are usually connected to individual pads with little or no sharing of test points. Implementing such structures over 10 or more metal layers turns into a problem of balancing the placement of the test structures and the pads for all those test points. The Scribe CV test chip proposed here will use two strategies to successfully manage an efficient trade off between pad and test structure placement.

First, test structures will be stacked vertically on top of each other like layers are stacked and used on every product chip. The pads for testing will only be implemented in the top metal layer, which leaves plenty of area for test structures to be buried underneath the pads. A symbolic cross section of this concept can be seen in Figure 1.

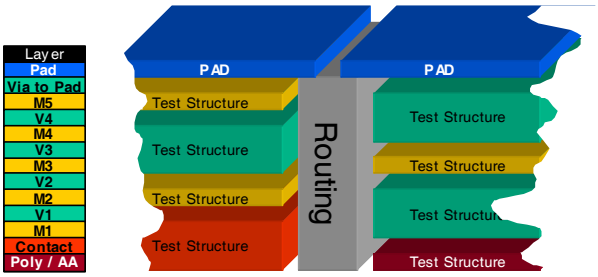

Figure 1: Concept of arranging stacked test structures under test pads.

Second, test points will be shared among test structures by multiplexing the test. For that, all available pads will be divided in two groups – drivers and receivers. Then, the drivers and receivers will be routed throughout the Scribe CV test chip in a way, that each test structure has a unique set of 2 drivers and 2 receivers to connect to within a subchip. Figure 2 shows a test structure bounding box of a subchip with 2 drivers being available in the upper left and

lower left of the box as well as two receivers being available in the upper right and lower right of the box. In this case a snake and comb test structure is then connected to those drivers and receivers. If an open circuit will interrupt the snake, the current flow between the upper left driver and the lower right receiver will be interrupted, and thus detectable through testing. If a short circuit will connect the snake with the right comb, the additional current will be measurable between the upper left driver and the upper right receiver. If a short circuit will connect the snake with the left comb, the additional current will be measurable between the lower left driver and the lower right receiver.

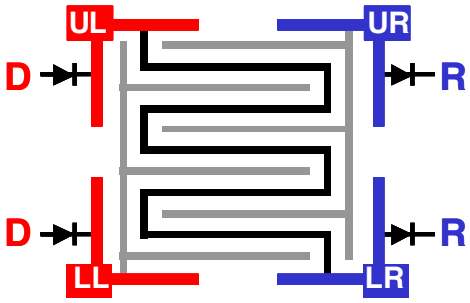

Figure 2: Placement & connection of a snake and comb test structure within a subchip

Figure 3 shows a test structure bounding box of a subchip with 2 drivers being available in the upper right and lower left of the box as well as two receivers being available in the upper left and lower right of the box. In this case two via chains are then connected to those drivers and receivers. A possible open circuit of the left chain can be measured between the lower left driver and the upper left receiver. A possible open circuit of the right chain can be measured between the upper right driver and the lower right receiver. A possible short circuit between the chains can be measured between the upper right driver and the upper right receiver.

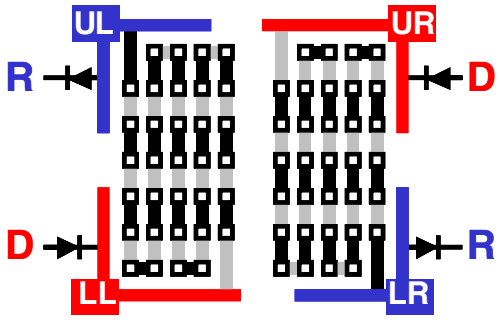

Figure 3: Placement & connection of a double contact/via chain test structure within a subchip

Simple diodes will be used as multiplexing devices. The arrangement is based on a simple diode array as for instance being used by [LiBL85], [WWGH92], and [WWRH90] to address 2 port test structures. It is then expanded to manage 4 ports per subchip as introduced by [HeWe94] and further enhanced and described in detail at [HILS06].

Figure 4 shows the top down design of the Scribe CV test chip. Starting point is a pad frame with for instance 50 pads on the left. For every 2 pads one subchip will be created underneath the pads. The routing will flow like a snake and comb around those subchips. In the horizontal routing channels a bank of diodes will be placed that allows a flexible assignment of diodes between the subchips and the driver and receiver pads. For each test structure, one driver and one receive will be available in the two horizontal routing channels adjacent to each subchip as required by Figure 2 and Figure 3.

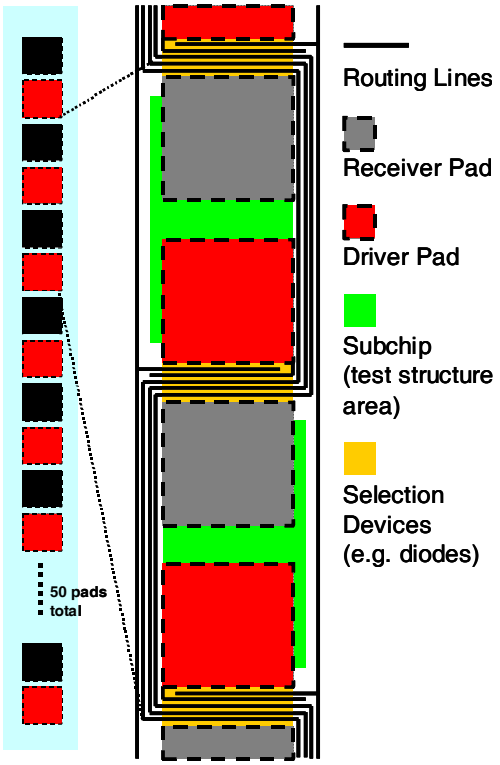

Figure 4: Arrangement of routing channels, test structures, and selection devices within the Scribe CV test chip.

Finally, the Scribe CV test chip will be placed within the scribe lines of product chips as illustrated in Figure 5. Here for instance 16 product dies are placed within a reticle. Four Scribe CV test chips have then be placed within the same reticle. Any particular number of placements can be chosen.

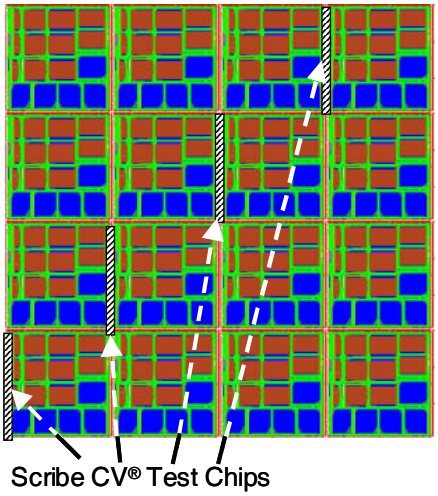

Figure 5: Example of Scribe CV test chip placement within a reticle of 16 dies.

3 Testing

Scribe CV testing utilizes a custom tester which is tuned to balance throughput against accuracy. There are 256 parallel force/sense channels and 16 supplies.

Figure 6: pdFasTest System

A fast, high resolution DMM is operated in a semi-fixed current range and is controlled in a tight s/w loop, utilizing h/w triggering. Additionally, by optimizing integration time and delays, we realize measurement times of ~3ms/meas. and a resolution of ~ 0.1uA. Overall test times are estimated to be 35x faster than a COTS (Commercial Off The Shelf) system.

Test System	# Meas./ wafer	Total test time / wafer
COTS	50000	160 min.[1]
pdFasTest®	50000	4.5 min [2]

Table 1: Test time comparison between pdFasTest and COTS Test System; [1]assumes 10,000 measurements per wafer can be executed within 32 min according to [AAN03] (keeping in mind that parallel measurements on multiple SMU's are not allowed due to layout considerations which require all measurements to be sequential); [2]Data from production runs

4 Experimental Results

Scribe CV test chips have been implemented in a 90nm SOI technology with up to 8 BEOL metal layers. Within the reticle scribe lines, a variety of PCM test chips are used beside Scribe CV test chips alongside with multiple product dies. Table 2 summarizes the test time differences. Within the same test time budget, about twice as many Scribe CV test chips can be tested.

PCM	Sites (die)	Test Time (min)	Add'l time (min)	Test time per site (min/die)
Non multiplexed test chip	9	3	0	0.33
	40	12	9	0.30
SCV (M4+M8)	36	9	9	0.2 + 1.75" load/unload
SCV (M8)	81	9	9	0.09 + 1.75" load/unload

Table 2: Test time comparison between conventional non-multiplexed PCM test chips and Scribe CV test chips.

The multiplexing of test structures further enhances the availability of experiments. Table 3 summarizes the available information per layer for a fixed test time budget. The numbers reflect the factor for available information from the Scribe CV test chip over available information from a non-multiplexed test chip. Looking for example at V1 opens, Scribe CV analysis data will be based on inspecting 111 times more vias compared to data based on a non-multiplexed test chip using the same overall chip area and the same overall test time. In general, Scribe CV shows superiority over open circuit related failure types taken from contacts & via chains and snake type test structures. In volume-production when test-time is a limiting factor, Scribe CV provides superior observability due to a much more balanced selection of test structures.

Process Module	Fail Type	M4+M8 with Site info	M8 with Site info
AA (RX)	OPEN	9.1167	10.2563
AA (RX)	SHORT	2.0152	2.2671
PO	OPEN	9.8901	11.1264
PO	SHORT	0.4853	0.5459
MC-AA	SHORT	1.6433	1.8487
MC-PO	SHORT	0.0475	0.0535
MC	OPEN		
MC	SHORT	1.5574	1.7521
M1	OPEN	6.0669	6.8253
M1	SHORT	0.5854	0.6586
M2	OPEN	3.6546	4.1114
M2	SHORT	0.3872	0.4356
M3	OPEN	5.0684	5.7020
M3	SHORT	0.5725	0.6441
M4	OPEN	2.8083	6.3187
M4	SHORT	0.3231	0.7269
M5	OPEN	1.8817	4.2339
M5	SHORT	0.2143	0.4821
M6	OPEN	1.5307	3.4442
M6	SHORT	0.3010	0.6773
M7	OPEN	1.4889	3.3499
M7	SHORT	0.8379	1.8852
AA-MC-Contact	OPEN	9.2494	10.4056
PO-MC-Contact	OPEN	4.9064	5.5197
AA Stack	OPEN	1800.0000	2025.0000
PO Stack	OPEN	1800.0000	2025.0000
V1	OPEN	111.2286	125.1321
V2	OPEN	126.3426	142.1354
V3	OPEN	44.7840	100.7640
V4	OPEN	61.4967	138.3676
V5	OPEN	118.5503	266.7382
V6	OPEN	8.6534	19.4702

Table 3: Comparison of available information for a fixed test time budget.

Figure 7 shows the comparison of parametric trends over several lots. Strong trends will be picked up equally well from Scribe CV test chips and non-multiplexed test chips.

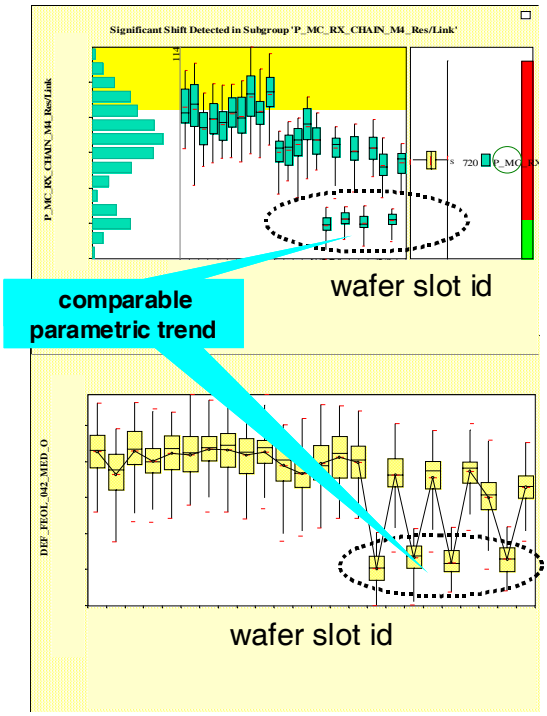

Figure 7: Comparison of detectable data trends from local interconnect chains between non-multiplexed test chips (top) and Scribe CV test chips (bottom).

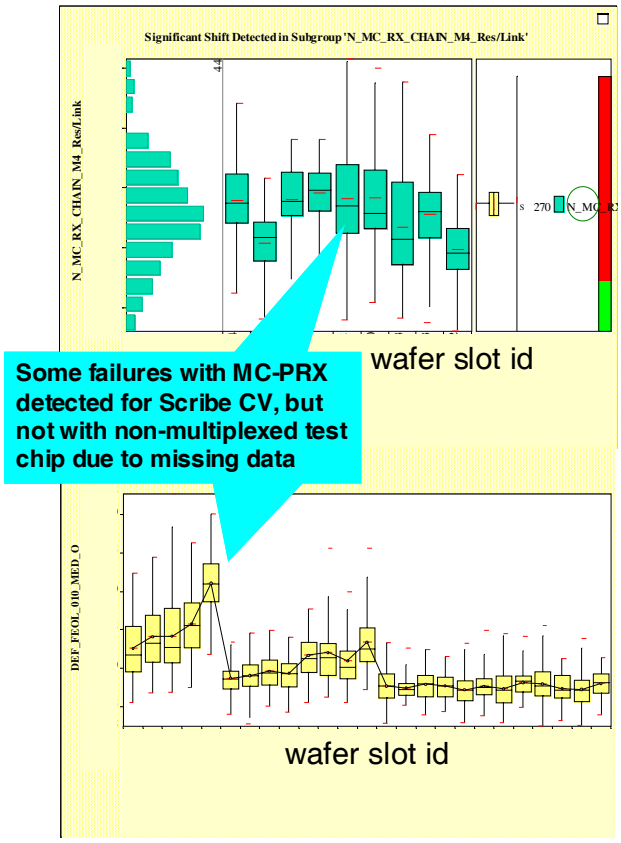

Figure 8: Data trend from local interconnect chains, which has been detected by Scribe CV test chips (bottom), but has been missed by non-multiplexed test chips (top).

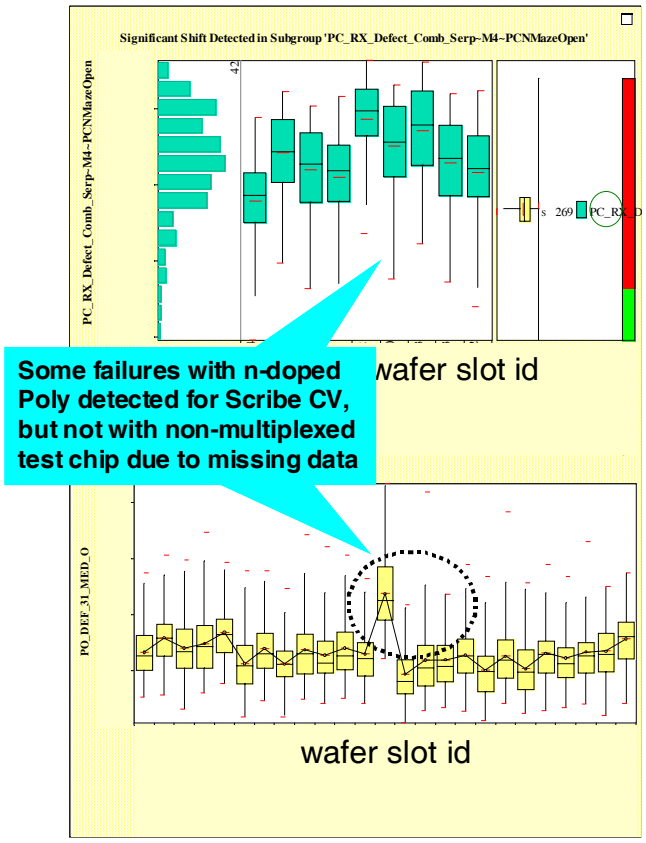

Figure 9: Data trend from n-doped poly snakes, which has been detected by Scribe CV test chips (bottom), but has been missed by non-multiplexed test chip (top).

However, softer signals, which only show up in a very small number of sites per wafer maybe easily missed by the non-multiplexed test chip as can be seen in Figure 8 and Figure 9. Such issues may happen either due to fact that less non-multiplexed chips will be tested per wafer or due to the fact that the observability for certain fail types is too low within the non-multiplexed test chip.

Scribe CV also serves as an excellent monitor for detecting the variability of layer specific resistance values taken from contact and via chains as well as from single layer snake structures. The combination of increased observability and large test coverage enables spatial trend analysis as shown in Figure 10.

Using Scribe CV data also enables a correlation analysis towards lot equipment history. For example, active area related data from Scribe CV have been used to determine which tool has caused certain findings and being the source of electrical variability. Figure 11 shows strong correlations between Scribe CV data from the FEOL module and tools from 2 process steps - “II dry resist strip” and “Spacer 2 resist dry strip”. The plots in Figure 12 and Figure 13 display module yield vs. the process date in a specific process step, split by different symbols representing lots processed in different tools. The legend for the symbols is to the right of the plot. The left side of the legend is a yellow boxplot of the module yield vs. each tool, rotated to a vertical orientation.

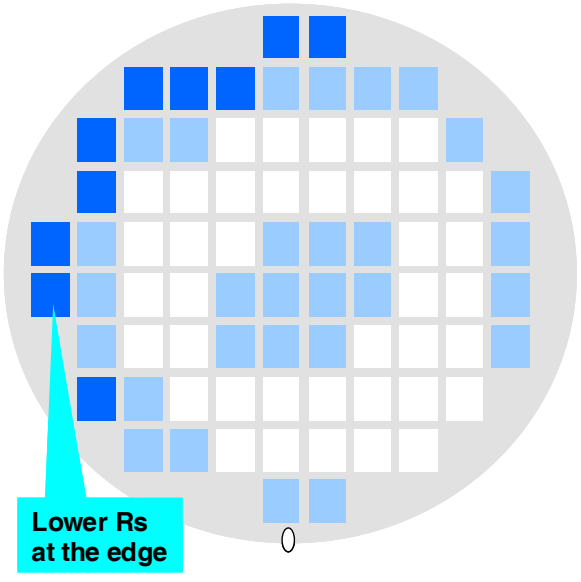

Figure 10: Detection of sheet resistance variability using Scribe CV data.

Figure 12 looking into the “II dry resist strip” process step shows one tool "DN02" stands out as having significantly lower yield. In case of the “Spacer 2 resist dry strip” process step, Figure 13 indicates tool “FH01” having significantly lower yield. To the left of the time trend is a histogram showing the distribution of the module yield for those two cases. Value bins in each histogram can be read from the Y-axis of the time-trend. Each histogram is split by color, according to the tool symbol legend.

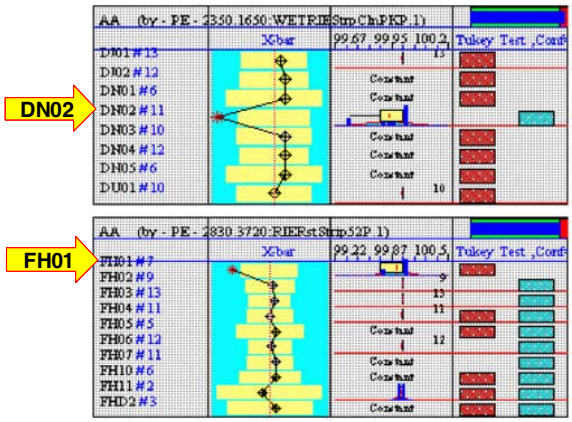

Figure 11: Correlation Analysis between Scribe CV data and lot equipment history data.

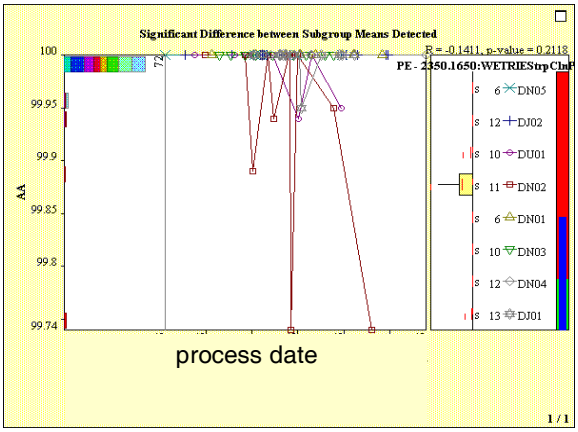

Figure 12: II dry resist strip tool data indicate issues with tool DN02.

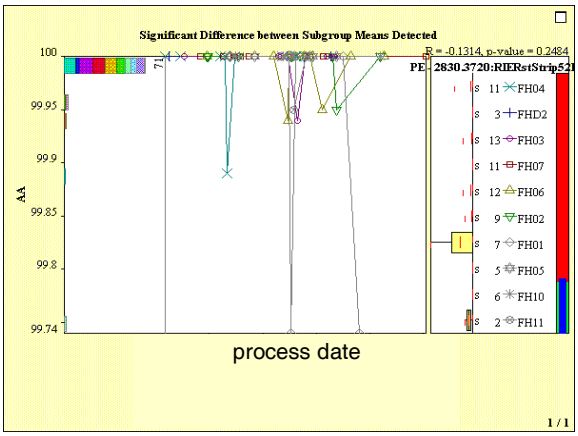

Figure 13: Spacer 2 resist dry strip tool data indicate excursions for tool FH01.

5 Conclusion

Compared to conventional non-multiplexed scribe line monitoring structures, the Scribe CV test chip based monitoring system provides significantly more data by maintaining the same area and test time budget. Scribe CV achieves an outstanding area usage and superior balancing of FEOL and BEOL experiments by stacking test structures on top of each other and packing them underneath pads. Its simple and robust multiplexing scheme ensures fast design time and minimizes misinterpretation of measured data. It is a very fast, robust and comprehensive yield monitoring system providing reliable and repetitive data. Due to its robust circuitry, data are available even during major yield crashes. Using pdFasTest enables testing of all sites per 300 millimeter wafer in less than 10 minutes including wafer handling time.

Analysis will be executed based on statistical methods for fast turn around and prioritization of potential processing issues. Defect densities (opens & shorts) and fail rates can easily be extracted due to a simple mapping between test data and test structure layout. Variability data about layer specific resistance values are also available, which are well suited for analysis of regional signatures. The increased amount of available data enables reliable correlation of scribe data with product data and lot equipment history logs. Also spatial trends and excursion wafers are detectable, even for mild excursions.

References

[AAN03] Agilent Application Note AN4070-5; Adapting Agilent 4070 series to open/short measurement of YIELD TEST CHIP; 2003

[Bueh83] Buehler, M. G.; Microelectronic Test Chips for VLSI Electronics; VLSI Electronics Microstructure Science, Vol 9, Chap.9, Academic Press, 1983

[DGGY05] DeBord, J. R. D., Grice, T., Garcia, R., Yeric, G., Cohen, E., Sutandi, A., Garcia, J., Green, G.; Infrastructure for Successful BEOL Characterization and Yield Ramp at the 65 nm Node and Below; Proc. IITC 2005

[DHLS01] Doong, K., Hsieh, S., Lin, S., Shen, B. Cheng, J., Hess, C., Weiland, L., Hsu, C.; Addressable Failure Site Test Structures (AFS-TS) for CMOS Processes: Design Guidelines, Fault Simulation, and Implementation; IEEE Transactions on Semiconductor Manufacturing, pp. 338-355, Vol. 14, No. 4, 2001

[HeWe94] Hess, C., Weiland, L. H.; Drop in Process Control Checkerboard Test Structure for Efficient Online Process Characterization and Defect Problem Debugging; Proc. International Conference on Microelectronic Test Structures (ICMTS), pp. 152-159, San Diego (USA), 1994

[HILS06] Hess, C. Inani, A., Lin, Y., Squicciarini, M., Lindley, R., Akiya, N.; Scribe Characterization Vehicle Test Chip for Ultra Fast Product Wafer Yield Monitoring; to be published at Proc. ICMTS 2006

[LiBL85] Lindner, H., Brauer, H., Lehmann, C.;Taschenbuch der Elektrotechnik und Elektronik; VEB Fachbuchverlag, 1985

[WWGH92] Ward, D., Walton, A. J., Gammie, W. G., Holwill, R. J.; The Use of a Digital Multiplexer to Reduce Process Control Chip Pad Count; International Conference on Microelectronic Test Structures 1992, San Diego / USA, 1992

[WWRH90] Walton, A. J., Ward, D., Robertson, J. M., Holwill R. J.; A Novel Approach for an Electrical Vernier to Measure Mask Misalignment; 19th European Solid State Device Research Conference ESSDERC ’89, Springer Verlag, Berlin, 1989

Biographies

Christopher Hess received the diploma degree in electrical engineering and the Dr.-Ing. (Ph.D.) degree in computer science from the University of Karlsruhe, Germany in 1992 and 1998 respectively. Since 1998 he is with PDF Solutions, where he currently serves as a Fellow being responsible for Yield & Performance Characterization. Since 1992, he has been involved in the design of more than 50 test chips and he holds 6 patents. Dr. Hess has published more than 30 conference and journal papers. He is a technical committee member of several semiconductor manufacturing related conferences and he has served as Technical Chairman and General Chairman of the International Conference on Microelectronic Test Structures (ICMTS) in 2000 and 2003, respectively.

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Hideki Matsuhashi received his B.S. degree from Tokyo University of Technology and Agriculture in 1993, and M.S. and Ph.D. degree from Tohoku University in 1995 and in 1998 respectively. He joined interconnect and packaging group in The University of Texas at Austin as a postdoctoral fellow in 1999. He had been involved in SEMATECH projects of study on reliability of Cu interconnect and low-k dielectric in large scale integrated circuit. He joined PDF Solutions, Inc in 2002, and he has been working as a senior yield ramp engineer.

Michele Squicciarini received his diploma in electrical engineering from the University of Brescia, Italy in 2000. He then joined STMicroelectronic's R&D - Timing Group, where he contributed to the study of the process variation impact on digital circuit performance. In 2003 he joined PDF Solutions where he currently working as an Analog Designer.

Ron Lindley received his MS in Physics from the University of Missouri-Columbia in 1979. For 5 years he worked in Bipolar process development and CMOS process sustaining at Burroughs Corp. For 7 years he worked in Reliability Test at Unisys Corp. For 7 years he has been working on Test Chip design and test at Cadence Design Systems, Inc. In 2001 he joined PDF Solutions, Inc., where is currently engaged in tester H/W development and sustaining.

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