Yield Learning Through Design Attribute Extraction

PDF SOLUTIONS

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1. Introduction

In the age of multi-billion dollar semiconductor fabrication facilities and increased time-to-market pressures, rapid yield learning is essential to achieve profitable production of integrated circuits (ICs). Even though IC manufacturers are well aware of the need for steep yield ramps, disaggregating yield loss into its underlying causes for a particular product in a given fabrication environment is difficult and time consuming. This task becomes even more formidable when using a single fabrication facility to manufacture multiple products or distributing the fabrication of a single product over multiple facilities. Fortunately, while both of these scenarios may make it more difficult to manufacture particular integrated circuits, they also offer a potential wealth of cross-correlation information that may be used to one's advantage [2][5].

It is often the case that multiple products running in the same fabrication environment yield differently. Even when a process has been well characterized, the yield for its products may not be sufficient. Moreover, when a product is transferred from one fabrication facility to another, its yield will change. Each of these situations confirms the intuitive notion that *design choices impact yield*.

This paper presents a methodology for *design attribute extraction* that enables designers and manufacturers of integrated circuits to determine, predict and possibly correct various causes of IC manufacturing yield loss. The discussion opens with a brief description of the philosophy behind design attribute extraction (DAE). DAE is a process in which selected attributes, or characteristics, of IC designs are extracted from its physical layout.This is followed by a few simple examples illustrating the application and potential benefits of DAE. Finally, the discussion concludes with pragmatic perspectives on the DAE process, including its software and input data issues.

2. Design Attribute Extraction

It is well known that the IC manufacturing process suffers from two main sources of yield loss: parametric variations and catastrophic defects. Within these two broad categories, however, a wide variety of underlying mechanisms are the actual perpetrators of manufacturing problems. These include but not limited to device and interconnect performance variation and electrically shorted, broken or otherwise malformed devices and interconnects. Recognizing that each yield loss mechanism may be stimulated by different electrical and/or structural attributes of a design suggests that *particular design attributes may impact yield* and that *designs with different attributes may yield differently.*

Design Attribute Extraction (DAE) is a process in which selected attributes, or characteristics, of IC designs are extracted from its physical layout. (The process may also be applied to schematic, functional and behavioral descriptions of a design; but for both clarity and brevity, these types of analyses are not presented here.) Examples of physical layout attributes that may be extracted include:

- the susceptibility of metal layers to contaminant-driven electrical shorts or opens (*i.e.* critical area [4][6])
- statistics concerning the geometrical dimensions and frequency of occurrence of various physical structures (*e.g.*, electrical device regions, interconnect layer components, certain processing layer stacks, etc.)
- measurement distributions of physical quantities exhibiting known systematic process variations (*e.g.*, ILD thickness variations due to chemical mechanical polishing, metal line width variations due to optical lithography, etc.)
- statistics concerning the physical structure of designed electrical nodes (*e.g.*, the number of vias per node, the distribution of metal line widths in each layer for each node, etc.)

Applying such an extraction process to a number of designs manufactured in a number of different fabrication environments can help answer the following questions:

- Why do some products have higher yields than others?
- Why do some product types have different failure modes than others?
- What are the important differences between those products?
- What are the important differences between the fabrication facilities in which those products are manufactured?

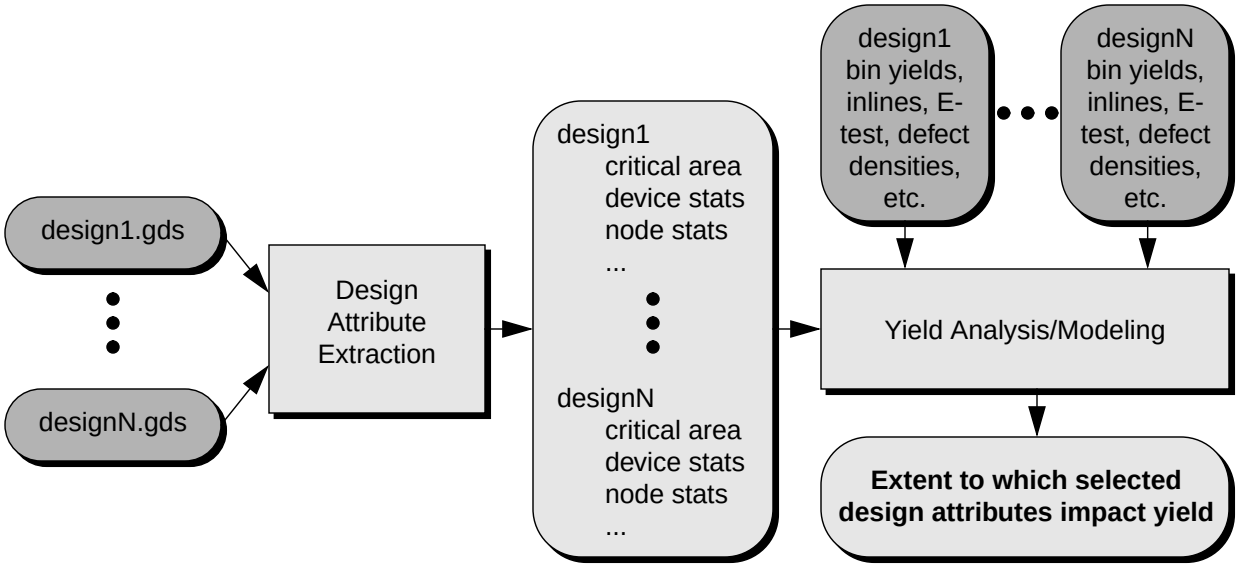


Figure 1. Overview of the Design Attribute Extraction (DAE) process and typical utilization of the design attribute data it produces. Rounded boxes denote data, rectangular boxes actions. User input data is further highlighted with darker shading to distinguish it from data derived during the DAE flow.

An overview of the DAE flow is shown in Figure 1. In this flow, attributes are extracted from a number of designs and correlated with associated manufacturing data (*e.g.*, product bin yields, in-line measurements, optical defect data, etc.) to infer which design attributes best model yield loss. Once known, this information can be used for various purposes, including:

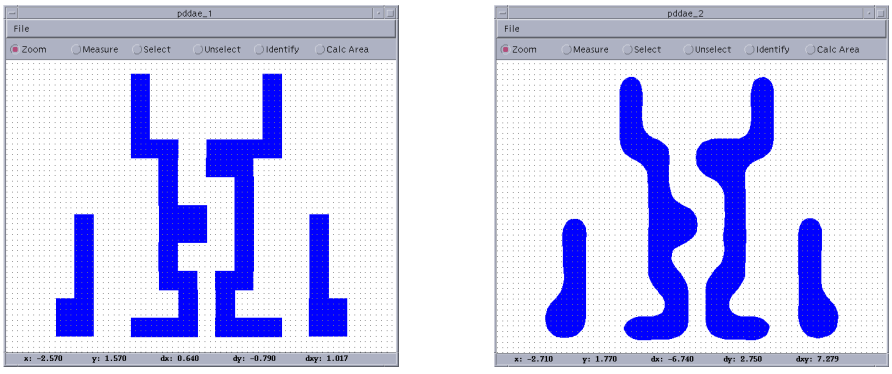
- narrowing the scope of possible cause(s) of yield loss for a particular design during yield ramp-up and production.
- predicting the yield of a design currently in production in one fabrication facility that must be transferred to another facility.
- predicting the yield of a design before it is committed to silicon using the designs' attributes as inputs to yield models from other designs already in production.

2.1. Process Modeling Considerations

Accurate extraction of design attributes may require a certain degree of fabrication process modeling. This is due to the fact that designed mask layers are not always accurate representations of the physical structures that are actually fabricated by the manufacturing process.

Obvious perturbations to mask layers include simple bloating or shrinking to account for the biasing effects inherent during optical lithography. Other, more time-consuming mask perturbations include aerial imaging simulation of optical proximity effects (OPE) and 2-D or 3-D simulation of etch agent microloading. Examples of OPE modeling are shown in Figure 2. Any number of such processing modeling steps may be required, depending on the sophistication of the manufacturing process as well as systematic mask perturbations performed after design "tapeout" (*e.g.*, optical proximity correction).

In light of these process modeling considerations, a generalized DAE methodology is shown in Figure 3.



(a) (b)

Figure 2. Models of the polysilicon gate layer for an SRAM cell. (a) shows the drawn mask layer, (b) shows the printed imaged as modeled by aerial imaging simulation.

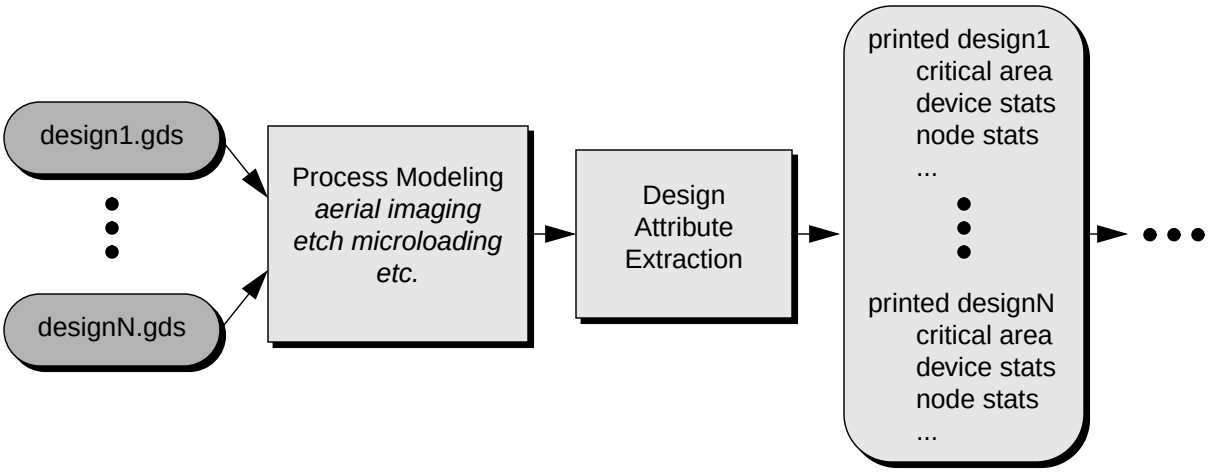


Figure 3. Generalized DAE methodology, including processing modeling to ensure that extracted attributes reflect true physical construction of design.

3. Examples

This section presents three typical applications of the design attribute extraction concept. Rather than provide an exhaustive discourse on the subject, these examples are intended to highlight important aspects of design attribute extraction and provide simple, concrete examples of the ideas presented in this paper.

3.1. Two products, defect-related yield analysis in the same fab

As stated earlier, it is commonly the case that two designs manufactured in the same "fab" yield differently. Among the possible yield loss mechanisms responsible for this difference, contaminant-induced bridging faults (*i.e.*, electrical shorts) are likely candidates [3]. Design attribute extraction can be used to test this hypothesis. In this application of DAE, salient attributes are extracted from each design and used to generate layer yield predictions. These yield predictions may then be analyzed in conjunction with true manufacturing yields to determine if each product's yield loss is primarily defect-driven.

Single layer critical area (for shorts) is a design attribute known to correlate well with a layer's susceptibility to bridging faults. (The critical area for a defect of radius *R* is defined as the area in which the center such a defect could fall and create a short between two or more different electrical nodes [5].) The DAE flow used to extract and analyze critical area is shown in Figure 4.

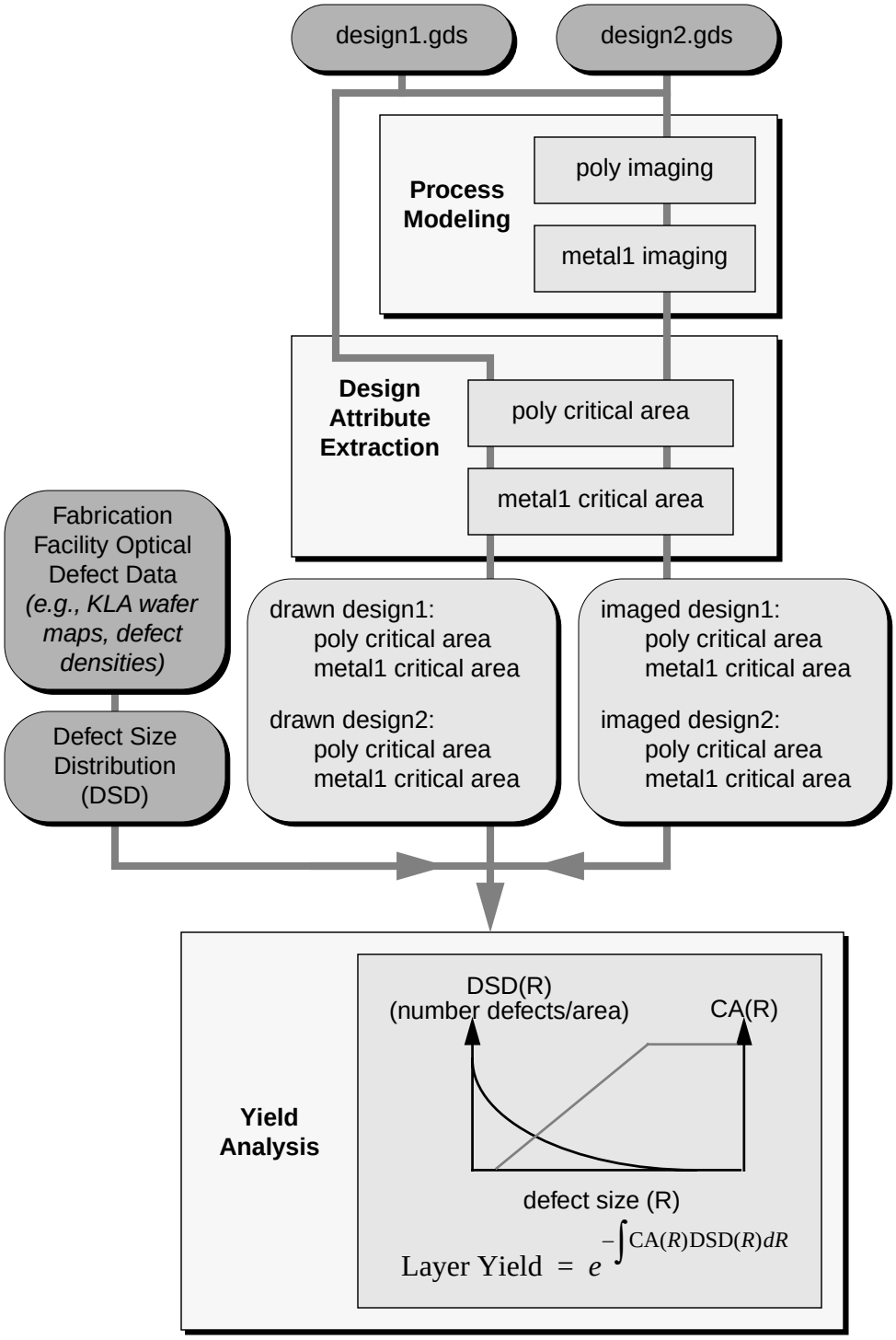


Figure 4. Task and data flow for critical area extraction for two designs, with and without process modeling. The end result of the flow is a set of layer yield predictions for the drawn and imaged models of the poly and metal layers of each design. (User input data is highlighted with darker shading.)

	Product A		Product B	
	drawn	**imaged**	**drawn**	**imaged**
predicted poly layer yield	99.02%	99.17%	97.37%	98.24%
predicted metal1 layer yield	97.89%	98.44%	95.43%	96.83%
product yield: (poly yield)(metal1 yield)*	96.93%	97.62%	92.92%	95.13%
predicted product scrap	3.07%	2.38%	7.08%	4.87%
scrap prediction error (drawn vs. imaged)	**+29%**		**+45%**	

Table 1. Results of DAE-based layer yield prediction for two 0.35µ digital designs.

Both process modeling and non-process modeling data-paths are shown in Figure 4 to highlight the need for the extra effort of process modeling. Consider the layer yield predictions in Table 1. These numbers were computed by applying the flow in Figure 4 to two 0.35µ digital CMOS logic products. Not only do these predictions support the fact that different designs have different susceptibilities to certain yield loss mechanisms (in this case bridging faults), but they also hint at the importance of including process modeling as part of the DAE flow. Specifically, scrap yield predictions using pure GDS-II files from the two designs are off by as much as 45% compared to predictions made after modeling the metal layers with aerial imaging simulation. The geometrical effects of aerial imaging simulation on critical area computations are illustrated in Figure 5.

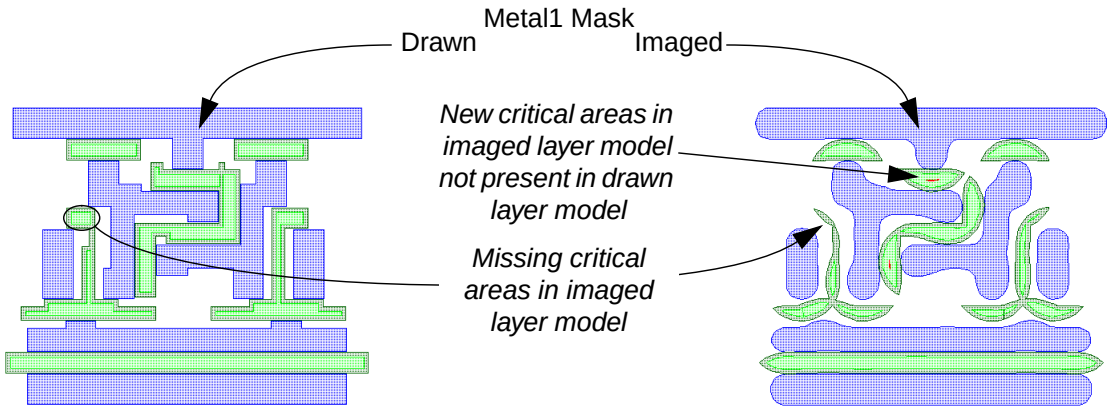


Figure 5. The effect of aerial imaging simulation on critical area predictions. The concentric contours shown in each plot represent critical areas for decreasing defect sizes. Not only do certain critical areas disappear when using imaged layers, other critical areas are created for smaller defect sizes due to bloating of wire end-stubs.

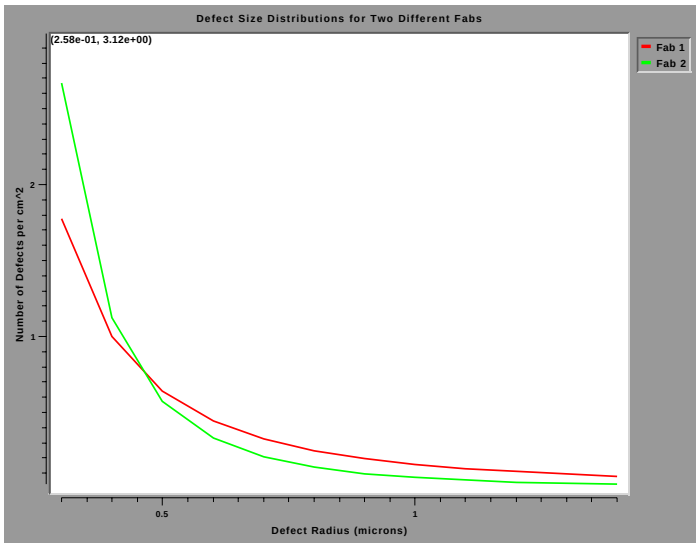


Figure 6. Defect size distributions for two different steppers. These distributions were computed using Stapper's $1/R^p$ model with $p = 2$ and $p = 3$ [7]. Note that the total number of defects in each distribution is constant.

3.2. One product, defect-related yield analysis in two different fabs

Building on the previous example, consider the case in which one product is manufactured in two different fabrication environments. It is likely that the product will yield differently between the two environments. Design attribute extraction may be applied to understand or predict this difference.

To limit the degrees of freedom in this example, consider that the only difference between the two fabs is the *defect size distribution* within their steppers, as shown in Figure 6. *Note that the total number of defects is held constant*. Predicted yields for product B from Table 1 are shown below in Table 2.

	Fab 1		**Fab 2**	
	drawn	**imaged**	**drawn**	**imaged**
predicted poly layer yield	97.37%	98.24%	98.64%	99.18%
predicted metal1 layer yield	95.43%	96.83%	97.91%	98.61%
product yield: (poly yield)(metal1 yield)*	92.92%	95.13%	96.28%	97.8%
predicted product scrap	7.08%	4.87%	3.72%	2.2%
predicted scrap differences between fabs	**~40%**			

Table 2. Predicted yields for Product B from Table 1 for two different fabs with defect distributions as shown in Figure 6.

3.3. Two products, differing metal1 pattern densities, interconnect performances

This final example demonstrates how design attribute extraction (DAE) may be used to help disaggregate the contribution of interconnect performance variation to speed bin yields. Of numerous factors influencing interconnect performance, inter-layer fringe and overlap capacitance variations are notable suspects. In turn, such variations are largely determined by inter-layer dielectric (ILD) thickness variations resulting from chemical mechanical polishing (CMP) [1]. The DAE methodology may be applied to test this hypothesis by first extracting design attributes which predict ILD thickness variation, then searching for possible correlations between these figures and product speed bin yields.

One design attribute known to correlate well with CMP-induced ILD thickness variation is underlying metal layer *pattern density* [8]. Dielectric deposited over regions of high metal pattern density tends to remain thicker than that deposited over regions of low metal pattern density after CMP planarization (*e.g.*, Figure 7). The pattern density at a point (x, y) within a metal layer is defined to be the total area of metal in the neighborhood of that point (*e.g.*, within $\pm 1\text{mm}$) divided by the total area of the considered neighborhood. A DAE flow to extract this attribute is shown in Figure 8. A specific process modeling step has been left out of this flow since the dominant process effects are accounted for in the ILD thickness versus pattern density input data.

Applying the flow in Figure 8 to the metal1 layer from two digital CMOS designs produces the pattern density distributions in Figure 9. Three features of these distributions are worth noting. First, the mean pattern density of each design is different. This may lead to a systematic difference in interconnect capacitance between the two designs, even though they are both fabricated in the same facility. Second, both distributions show almost a 30% spread in pattern density. This variance leads to a spread in interconnect capacitance, and therefore delay, possibly causing unanticipated skew in designed signal paths. Third, the shape of each distribution is different. The distribution for Product B has a conspicuous tail toward low pattern density, indicating that process-induced delay skew may not affect all designs identically.

The ability to extract design attributes and predict interconnect performance variations offers design engineers the opportunity to analyze the robustness of their design *before* tapeout, and empowers production engineers with the ability to diagnose interconnect performance problems later on.

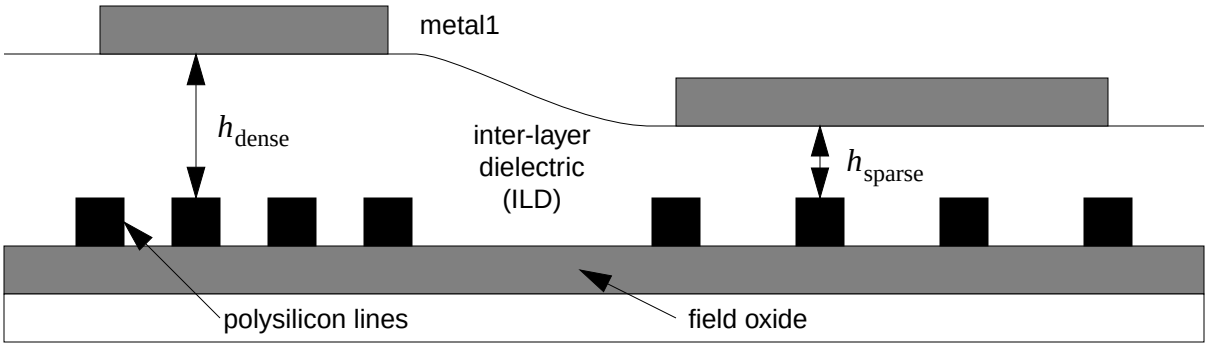


Figure 7. The effect of material pattern density on overlying dielectric thickness planarized by chemical mechanical polishing.

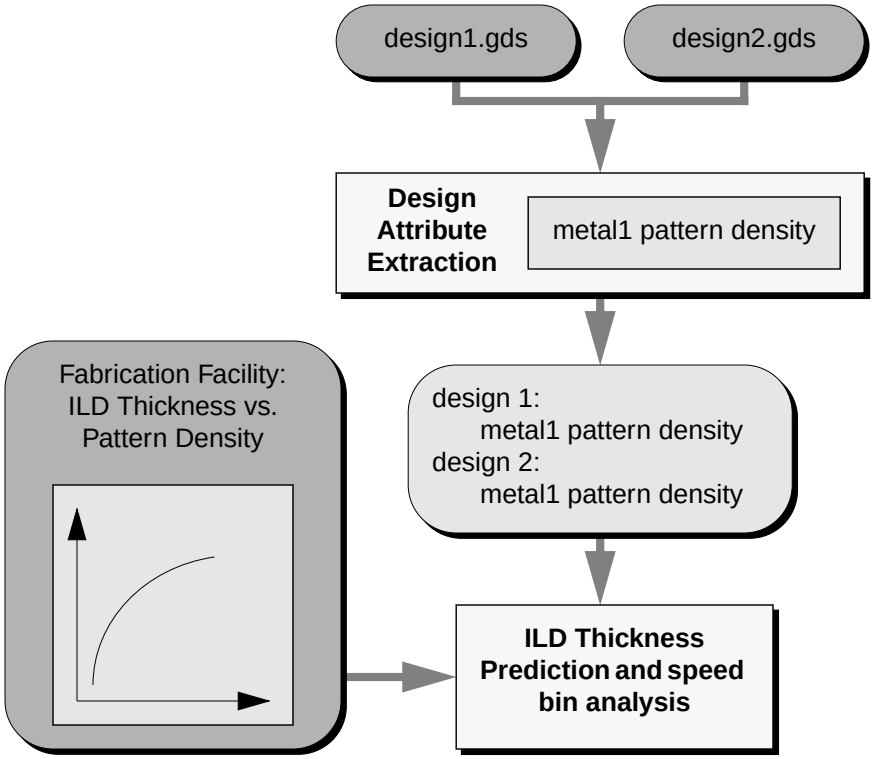


Figure 8. Task and data flow for metal1 pattern density extraction.

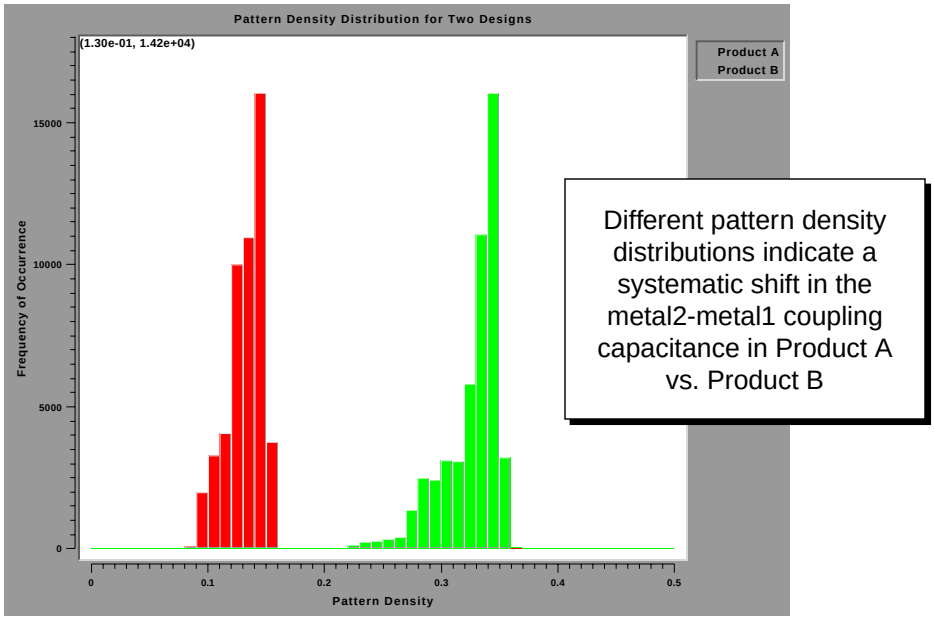


Figure 9. Metal1 pattern density distributions for two designs. Not only is the mean value different for each design, but also the shape of the distribution (notably the left-hand tail for Product B). Pattern densities were computed on a 10μ grid with a neighborhood distance of 1mm.

4. Pragmatic Perspectives on Design Attribute Extraction

While the concept of design attribute extraction enjoys an intuitive appeal, a number of important issues must be recognized before the benefits of DAE can be realized in practice. These issues include usability and audience considerations, input data requirements, and the need for a software architecture that is both easy to use and can handle the huge layout databases prevalent with modern designs.

First and foremost, design and production engineers should not need to know how to use the low-level software required to extract most design attributes. Insulating the user from this burden widens the potential audience and therefore applicability of the DAE concept. Proper construction of a DAE system will allow even weakly-computer-literate engineers to predict and analyze design attributes for their own unique purposes.

Second, a DAE system must have relatively simple methods for specifying input data and storing output data. Using the example flows from Section 3, the following are useful guidelines:

- Mask layout data should be readable from a number of formats, including GDS-II stream format and possibly direct access to vendor-specific databases such as Cadence Design Systems' Design Framework II.
- Manufacturing data should be easily accessible from within the DAE system. This includes not only electrical test, optical inspection and other in-line measurements, but also post-processing data such as wafer probe and package test yield figures.
- Extracted attributes from multiple designs and multiple technologies should be easily accessible from post-DAE yield analysis algorithms. Flexible access to extracted attributes affords the greatest possible opportunity for yield maximization through design attribute cross-correlation.

Third, in addition to providing extraction algorithms for well known design attributes, a DAE system should provide primitive operations from which a user can easily build their own extraction flows. It is undoubtedly the case that individual design and product engineers will have the firmest grasp on which design attributes are most important. A robust DAE system is most likely more a *tool box* rather than a *black box*.

Fourth and finally, a DAE system must be able to process large layout databases. By its nature, design attribute extraction and concomitant yield analysis is highly applicable toward leading edge designs which are difficult to manufacture. Often these designs are millions, or even tens of millions, of transistors. Therefore, a robust DAE system is most likely an open framework in which the most capable software can be used for each extraction task, including commercially available design rule checkers, layout parameter extractors and process simulators.

Figure 10 diagrams the block structure of pdEx (Process and Design Explorer), a software by PDF Solutions, Inc. The main purpose of pdEx software is to provide semiconductor manufacturers with tools to help disaggregate product yield loss mechanisms by encapsulating the technical tasks of DAE within a simple and extensible framework. The flexibility and generality issues

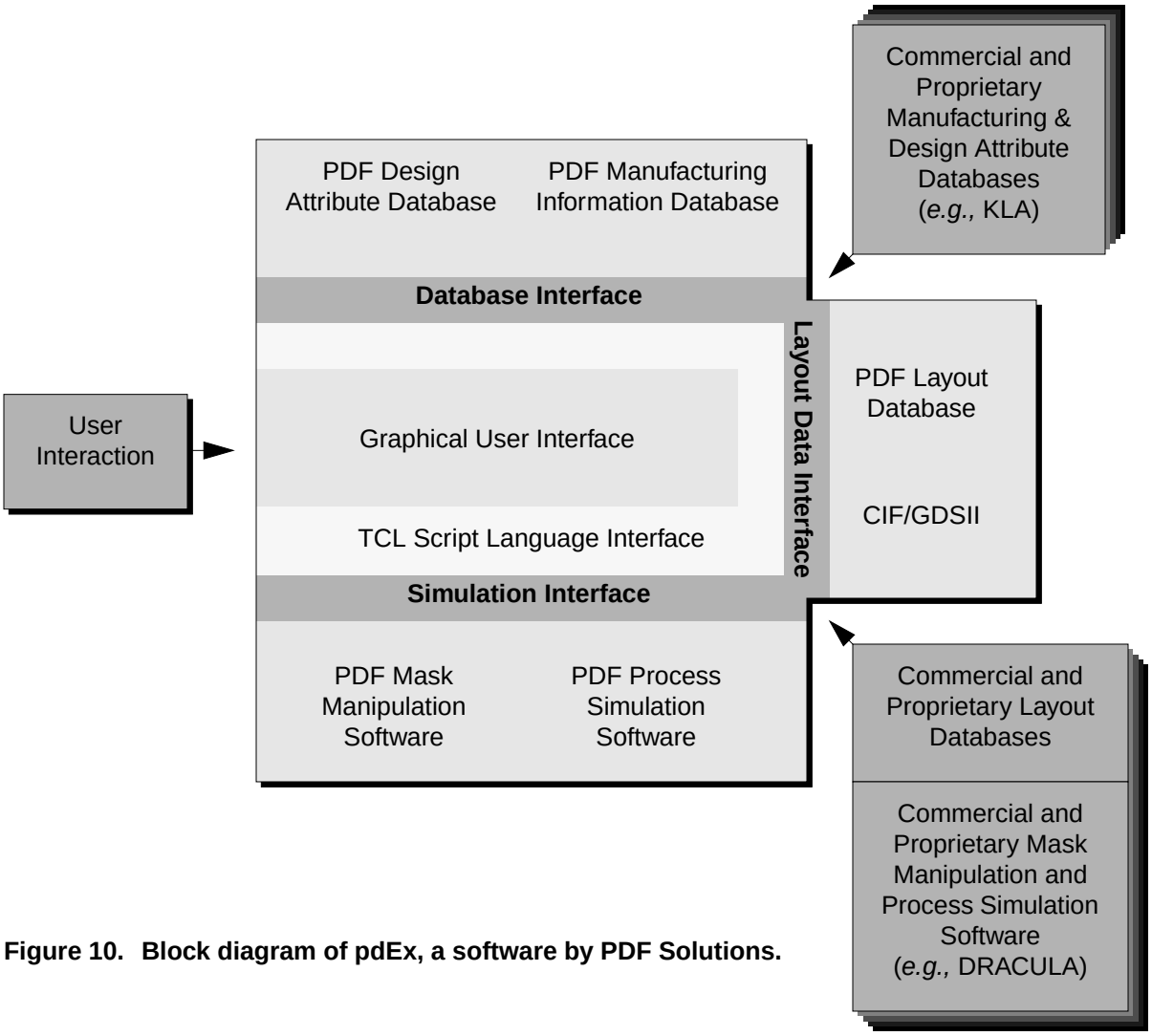


Figure 10. Block diagram of pdEx, a software by PDF Solutions.

detailed above are addressed by the various interface layers in the system. Of particular interest is the use of Tcl/Tk for the graphical user interface and low-level-tool scripting functions. This powerful software language allows the system to encapsulate its various functions and satisfy both the ease of use and modularity requirements specified above. Also of interest is the simulation interface. In addition to providing a generic API between attribute extraction algorithms and mask manipulation programs, the simulation interface also manages “windowed simulation” of large layouts.

5. Summary

With critical dimensions fast approaching the physical limits of VLSI fabrication technology, integrated circuits are becoming increasingly difficult to design and manufacture. This paper has presented a broad overview of the design attribute extraction (DAE) methodology for IC manufacturing yield analysis and prediction. Through DAE, IC designers and manufactures are given the ability to predict yield during the design phase and diagnose cross-product and cross-fab yield problems after production starts. Though still a new concept, DAE is enjoying increased interest

in the IC manufacturing community. pdEx, a software by PDF Solutions, encapsulates the technical tasks of DAE within a simple and extensible framework. Interested readers are encouraged to contact PDF Solutions for more information.

6. References

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