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Method for fast and accurate calibration of litho simulator for hot spot analysis

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Abstract – Deploying OPC that is robust over the process window is becoming more and more challenging as geometries shrink[i,ii]. This challenge has a major impact in time-to-market and yield of new products. This paper describes a litho simulator calibration flow using a streamlined OPC verification methodology. This new methodology successfully bridges design and manufacturing to accelerate the OPC development process and proactively identifies weak OPC locations that can reduce yield. The method includes an accurate simulator calibration using automatically obtained 'on silicon' measurement data, followed by full-chip litho simulation using the calibrated model to identify potential hot spots on product. The method also enabled a short cycle feedback loop to the OPC model generation resulting in improved OPC optimization and verification.

INTRODUCTION

As design rules shrink to 65nm and 45nm technology nodes, there has been an unavoidable increase in the complexity of OPC/RET schemes to enable printability. In addition, the greater probability of OPC errors often requires masks to be reworked or replaced and extends the time for OPC/RET qualification.

This paper describes a streamlined litho simulator calibration flow for OPC verification that successfully bridges design and manufacturing to accelerate the OPC development process. We examined two alternative methods for calibrating the litho models: the first measured 60 different structures while the second used a proprietary test chip and an automated metrology sequence created directly from the test chip design file in which 300 structures were measured on 5 different focus exposure fields. After calibration, a full chip simulation predicted locations which were likely to cause yield issues (hot-spots). These hot-spots were then verified on the printed wafer.

By using this integrated method to bridge layout and data collection, users realized a 3X time savings to qualify and optimize the lithography simulator calibration, equating to many days or even weeks of time[iii]. At the same time, the off-line recipe generation capability saved about a week of CD-SEM engineering time. In addition to identifying 'hot spots' that were missed using standard OPC verification methods, this method enabled rapid root cause analysis and offered timely feedback to the OPC model generation process.

LIMITATIONS OF CURRENT METHODS

Lithography process models must be accurately calibrated against experimental data before a reliable, robust OPC model can be successfully created to verify a layout. Verification entails extensive data collection covering a vast set of structures of varying sizes, shapes, and combinations of layers. However, in typical calibration methods, the OPC models are calibrated against a very limited set of structures due to time constraints including tool availability and engineering analysis time. In addition, even a well-calibrated model created with this method can miss certain product layout attributes specific to a particular product.

Current calibration data typically uses limited 'on-silicon' measurements because it relies on manual measurement recipe set-up which limits the number of measurements that can be taken. Roughly 60 measurements are typically taken per die, or per wafer. Having fewer calibration data points, and therefore a limited structure set to build the litho calibration model, can significantly impact model quality. Another drawback of manual measurement recipe set-up is the long turnaround time; it can take up to several weeks to obtain a complete data set of 60 measurements on 3 dies per layer.

In many semiconductor companies, the OPC and the metrology are performed by different organizations. The OPC/RET group and the Metrology groups may even be located in different cities. The lack of an industry standard format also contributes to OPC calibration measurement errors. For example, CD metrology measurements may be done on the wrong location or structure as a result of human errors in communication among different groups.

These limitations in turn limit the validity of the lithography model's prediction of actual product layouts that is so crucial for accurate verification. The gap between the need for large numbers of calibration structures, the large measurement dataset and actual calibration can be overcome by an innovative method for fast, automated calibration turnaround. Thie method accommodates the large data requirements for accurate modeling of across-field and across-wafer spatial variations, enabling it to predict the correct layout response. Fast, accurate calibration is an absolute requirement to verify on-product layout after OPC/RET corrections during the design, but prior to manufacturing, as part of a comprehensive DFM strategy.

Using OPC-Check WITH PDF CV Test Chips

This section briefly describes the methodology for the litho calibration using the OPC-Check on PDF CV test chips specially designed to capture printability related issues[iv] using the PDF PSD™ (Printability Space Decomposition) methodology.

Printability Space Decomposition

PSD is a PDF Solutions Inc. patented methodology for detecting printability-related issues prior to manufacturing. Figure 1 below captures a typical lithography process on a wafer stack. The objective in PSD is to evaluate the layout response to the litho process using a phenomenological model to assess the final post-litho or post-etch 'on silicon' behavior of layout features for manufacturability.

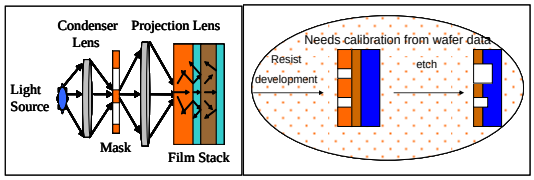

Figure 1. Representation of a typical lithography system on the mask and wafer stack.

In PSD analysis, a simulation is performed over an entire product layout across the process window for key process parameters, including exposure, defocus, mask effects, misalignment, and multi-layer effects. PSD also simulates the interaction combinations of all of these parameters. The output includes comprehensive statistics of yield-relevant attributes across the process window, and locations of potential process-related issues or defects. PSD requires a robust, accurate litho model. The OPC-Check tool was used to make the multiple measurements required for accurate models.

Verification with SEM

Accurate OPC models need to be calibrated with physical measurement data from a printed wafer. Relevant structures are printed under different processing conditions, then measured to assess sensitivity to process variations. Whereas process monitoring applications require high precision and are less dependent on absolute accuracy, measurement accuracy is critical for calibration, and becomes more demanding as tolerances shrink. Current CD-SEMs can achieve the accuracy on isolated lines necessary for the 22nm technology node[v].

OPC-Check overview

Applied OPC-Check is a bridge between EDA tools and the CD-SEM to facilitate the collection and reporting of metrology data. A file containing the instruction set required for the CD-SEM measurements, called DBM-Profile, is sent from the EDA tool and used by OPC-Check to automatically generate a recipe for the CD-SEM. This automated recipe creation capability replaces the traditional method of manually selecting alignment and measurement targets. The recipe can be ready for immediate execution upon wafer arrival and overall turn-around time from wafer to metrology results is reduced from weeks to days.

DBM-Profile provides a standard protocol for the metrology location(s), the type of measurement, and GDS image clips from the desired metrology sites. DBM-Profile facilitates communication across functional groups (RET and Metrology), and between companies (e.g., Fabless and Foundry). In this study, as illustrated in Figure 2, DBM-Profile offered a platform for error-free communication between multiple organizations (PDF, Applied Materials, Infineon) in the US and Germany.

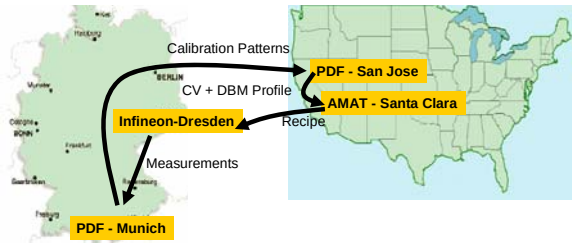

Figure 2. Data flow Error-free communication was possible using a well-defined DBM-Profile protocol:

PSD Litho Calibration Flow with OPC-Check

The recipes for about 1500 CD measurement sites per wafer were generated off-line from the VeritySEM measurement tool. The larger data set has benefits such as:

- Exploration of a wide layout configuration space,
- The ability to address across-field variability and process window;
- Improved redundancy in the data set; and
- Better validity for products layout simulation.
- The PSD litho calibration flow using the OPC-Check on the VeritySEM is shown in Figure 3.

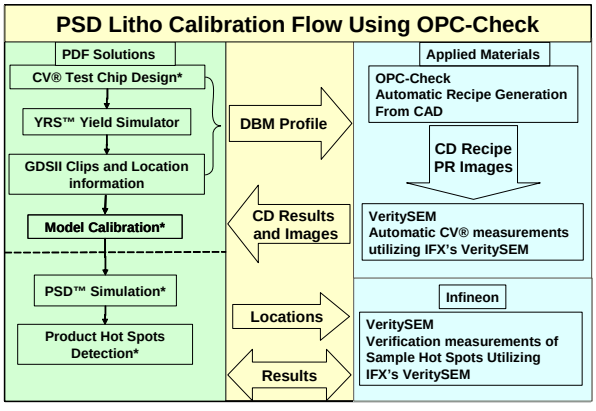

Figure 3. PSD™ Litho Calibration Flow using the AMAT OPC-Check® and VeritySEM™

The CV test chip is a full-reticle test chip comprising multiple layout patterns typical of product layouts. A detailed design of experiments (DOE) establishes the electrical characterization of the process. Several "hard to print" structures are included on the test chips specifically to monitor the printability process window. The calibration structures selected for automated calibration include 1D and 2D structures to capture the proximity curves, MEF (mask error factor) and 2D phenomena such as line end pullback, island printing, and line narrowing due to sparse or dense neighbors. The structure information relevant to calibration is imported into the YRS™ (Yield Ramp Simulator) software to automatically generate GDS clips of the structures and export an xml-based DBM file to OPC-Check. The OPC Check tool then generates the recipe, which is loaded into the VeritySEM system for automatic measurement of the processed silicon at the client site.

The measurements are used to calibrate the PDF optical simulation software (OPTISSIMO™) against the set of structures to create the fully calibrated litho model for the PSD analysis. The calibrated simulator is then used to run a simulation on the full chip layout. The result of the PSD analysis are litho-sensitive 'hotspots' in the product layout. The hotspot locations are verified by in-situ measurements using the VeritySEM.

RESULTS

The model calibration results shown here are based on measurement data from Infineon's 90nm technology for the active layer. The optical parameters for the active layer are 193 nm wavelength, 0.72 aperture and circular illumination with sigma 0.6. The optical parameters of the wafer material stack were available and used for the optical simulator calibration and simulations.

Hotspot results and SEM data are for the poly layer from Infineon's 90nm technology. The optical parameters for poly were the same as for active (193nm and 0.72 aperture) except that the poly layer used annular illumination with 0.7, 0.4 sigma. Material stack optical data were used in the model calibration and the hotspot simulations. The hotspots shown are based on full chip simulations.

Calibration results

The litho simulations were done with the OPTISSIMO optical simulator and proprietary resist model. The optical simulator is a kernel-based, aerial image simulator, capable of high NA simulation and includes wafer material stack effects.

An experiment was performed to illustrate the importance of a broad set of calibration structures. First, only a subset of the available dataset was used for calibration. This subset consisted of about 60 different lines-space 1D structures representative of what is commonly used to calibrate OPC simulators. The resulting model from the limited data set was labeled "conventional OPC model."

In a second calibration, all of the available structures and measurement data were used. This included numerous proprietary 2D patterns, such as 'notched lines' (not shown for space reasons). The resulting model was called "enhanced model". The total number of structures used for this model was about 200 structures per die. The "verification model" was then used to verify the predictive quality of the "conventional OPC model" on all available test patterns, including the 2D patterns.

Figure 5 shows the comparison of these two models. One can clearly see distinctive peaks in the graph where the models do not match very well, with differences in CD up to 20nm. These peaks correspond exactly to the 2D patterns that were left out for calibration of the "convention model", while the 1D patterns from both models produced very similar results.

We can conclude that, first, the OPTISSIMO resist model is capable of fitting 2D structures, without loss of accuracy in 1D structure patterns. Second, one can build a calibration model that does not predict 2D structures well. Therefore, having measurement data for 2D patterns is necessary to verify the quality of the model for these structures.

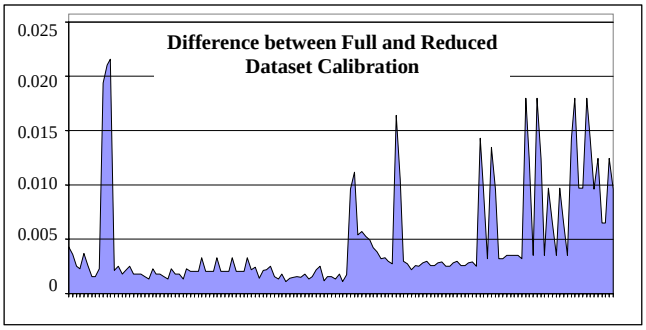

Figure 4. Difference between conventional OPC model and enhanced OPC model. The Y axis shows the difference in CD between these 2 models, X axis indicated different pattern types. Total number of patterns is about 200.

Hotspots on Field Poly

An important type of hotspot identified on the poly layer is a landing pad connected to a poly line by a short, minimum design rule-wide piece of poly. Typical OPC implementation leaves these connecting lines relatively narrow to compensate for the rounding of the inner corners. The sensitivity to defocus, as well as mask error, is one of the highest in the entire layout, drastically narrowing the overall process window of the product. SEM images of the hotspot location confirmed the relevance of the hotspot identified by the PSD analysis, as shown in Figure 6.

The observed defocus window matched the simulations well. Note also that the simulation comparison to experiment were based on post-litho development measurement data, while the SEM images shown of the hotspot location were from a post-etch wafer. Given the differences, the observed 'on silicon' necking and the observed defocus sensitivity supported the finding of the simulations. There were several possible solutions to improve printability of this hotspot as follows:

- Change in design. Since the poly connection line was not close to any active area, and therefore did not behave as a transistor, there was no reason to make its width the minimum design rule. A wider drawn line would immediately solve the problem.

- Change in OPC algorithm. An OPC setup that considers the process window of the correction was likely to help here. Also, specific code in the OPC algorithm for these kinds of design situations might result in a wider post-OPC connecting line and solve the problem.

Because of the timely feedback of the findings and recommended solutions, Infineon chose to change the OPC model. The revised OPC implementation had a significantly wider line at this location and other similar locations in the layout, effectively removing this type of hotspot.

The "S-shape poly" hotspot has a similar failure mode to the "T-shape" poly hotspot discussed above. In this case, due to the model-based OPC compensating for rounding at the inner corners and using a finite segment size modify the feature, the resulting width of the corrected poly in the center of the "S" bend was relatively thin. Again, as with the "T-shape poly," no scatter bars were possible at this site, increasing the defocus sensitivity of this location. The result was a narrow process window for manufacturing.

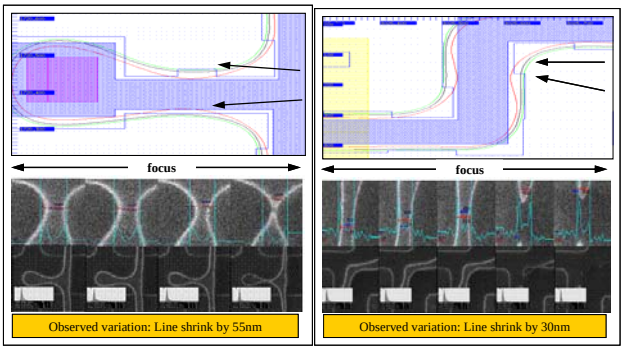

Figure 5. Hotspot examples: T Shape Poly (left) S Shaped Poly (right)

The SEM images shown in Figure 6 confirmed the location and magnitude of the simulated necking identified by the PDF PSD analysis. Note that the measurement data on the simulations were taken from post-litho development measurements, while the SEM pictures were taken from a post-etch wafer of the same hotspot location. The timely feedback of the PSD analysis and the verification 'on silicon' were important steps to initiate the revision of the OPC implementation. The revised OPC model eliminated this type of hotspot, resulting in a wider process margin.

Hotspots for Poly Gates: Gate Shrink on narrow width transistor

In the case of transistor structures, the sensitivity to process variations is very important. The effect on poly line width of a "worst case" line shrink condition due to a combination of exposure variation, defocus and mask error, is about 3 times higher than that of a isolated poly line. Although not shown here, our SEM images showed good agreement with the simulated process window from PSD analysis. As before, the measurement data on the simulations were taken from post-litho development measurements while the SEM pictures were taken from a post-etch wafer of the same hotspot location.

SUMMARY AND CONCLUSIONS

The use of automated OPC-Check allows for the off-line recipe generation for a large number of sites for CD measurement, leading to improved litho model quality and the ability to identify hot spots missed during nominal OPC verification. For manual set-up the practical limit is around 50-150 sites per wafer, while this method allows several thousand measurements. Having 10x more available measurements allowed exploration of "second order" structures, plus process window and across-field variability measurements.

The automated methodology also reduced cycle-time by linking test chip design, CD-SEM recipe generation and final measurements. We estimate a time savings of ~40 hours or more per measurement layer on the VeritySEM tool due to the off-line recipe generation; overall, the time required to calibrate the litho model decreased by approximately 3x. This methodology identified hot spots missed during the original OPC verification. This fast feedback was critical to meeting production demands.

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