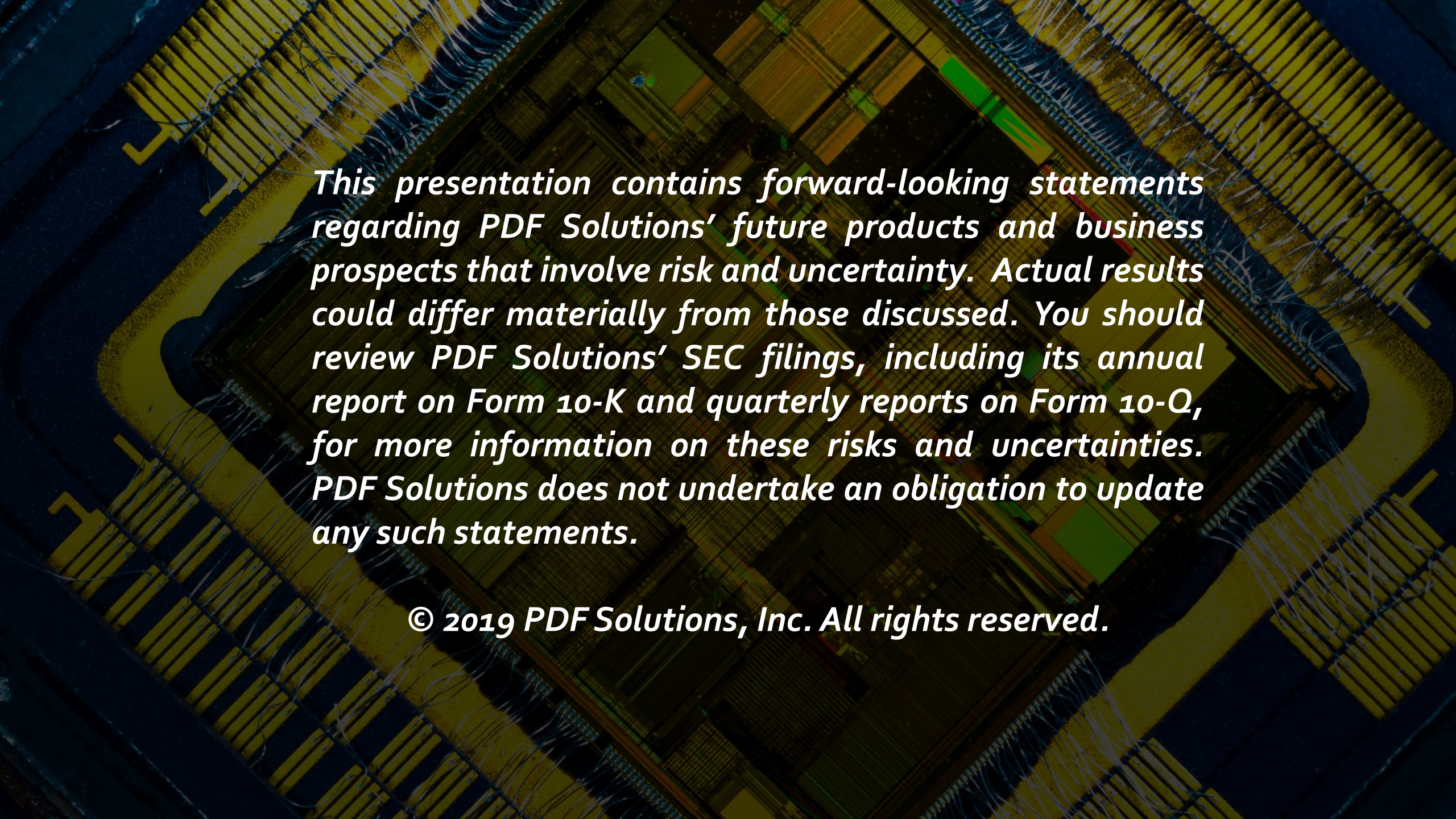
16th Annual
PDF Solutions
Users Conference

PDF/SOLUTIONS™

S1.4 – DFI™ and other New Sources of Data for Yield, Reliability and Process Control

October 15, 2019

Dennis Ciplickas, VP of Characterization Solutions



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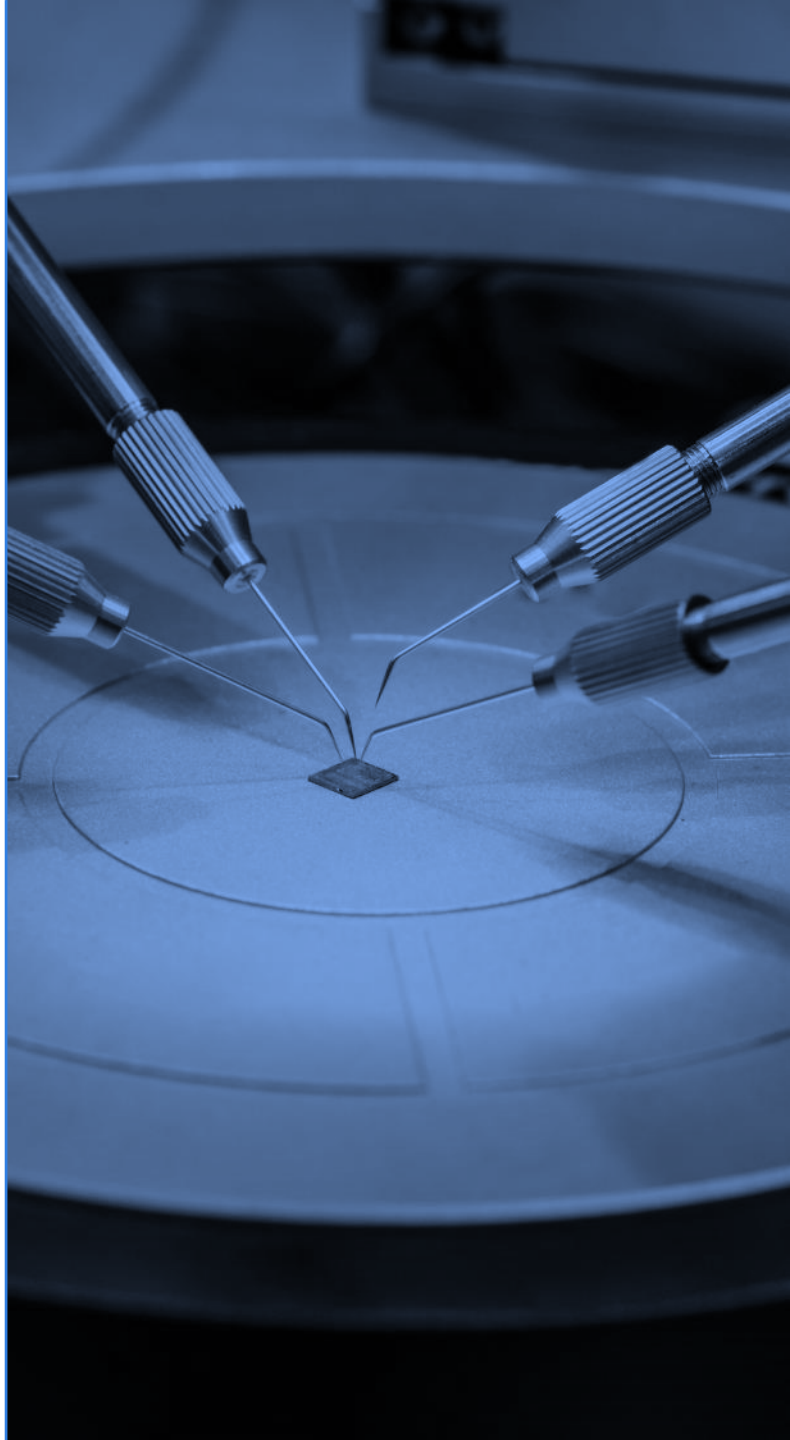
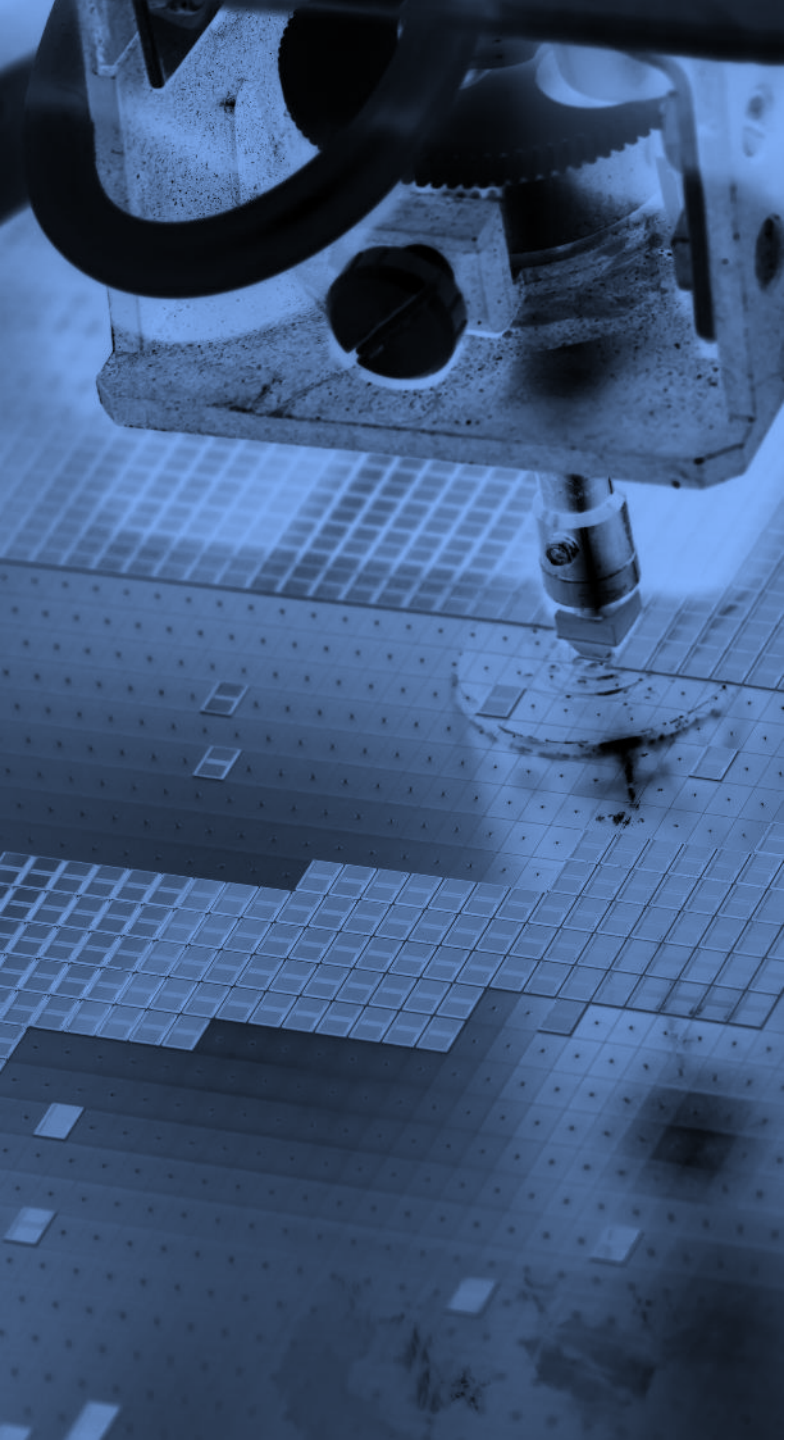
Introduction

- PDF's business has always been based on data
- Deep insight from the unique data generated by our Characterization Vehicle® (CV®) Infrastructure is a key enabler for time-to-market in our Integrated Yield Ramp (IYR) business
- As PDF's analytics business has grown, so has the complexity of semiconductor systems, and the need for unique data persists
- We are extending, re-inventing and re-deploying IYR technology to create synergy with Exensio® analytics and new offerings for the evolving semiconductor ecosystem





Industry Trends

- Automotive
  - Advanced Driver-Assistance Systems (ADAS)
  - Aggressive move into advanced technology nodes
  - Functional Safety
  - Quality
- Data center
  - New computing architectures
    - CPU, GPU, AI, in-memory computing
  - New memory and storage architectures
    - SRAM, NVM, DRAM, NAND FLASH, HDD
  - Power consumption, Power vs. Performance vs. Reliability tradeoffs
  - Uptime, SLAs
- Mobile
  - Small, dense form factors with advanced packaging
    - InFO, CoWoS, FOWLP, EMIB, etc.
  - 5G networking creates technology platform with need for more storage

Quality Driver: Automotive Electronics

1950
1% of total vehicle cost is electronic

2010
30% of total vehicle cost is electronic

Est. 2030†
50% of total vehicle cost is electronic

5,000
semiconductor devices per average car

1ppm failure rate = 5 failures every 1,000 cars

10,000 cars manufactured per day
= **2** failures each hour!

Key industries moving to ppb quality levels!

† statista.com

Power and Performance vs. Reliability

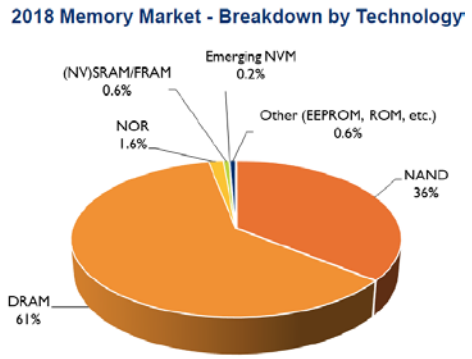
- Data Centers consume 3% of total electricity TODAY! †
  - Facebook: 100MW data center with 442,368 servers††
  - Facebook: average server utilization ~40% (265,420 unused servers) ††
- AI: Rat brain 518,400 processors, human brain 1000x more performance needed ††
- Poor Reliability leads to Silent Data Corruption, unacceptable latency and lost revenue
- New technology is needed to…
  → …achieve 10x lower power to continue growth
  → …enable reliability that meets aggressive SLA commitments

† forbes.com †† FLASH Memory Summit 2018

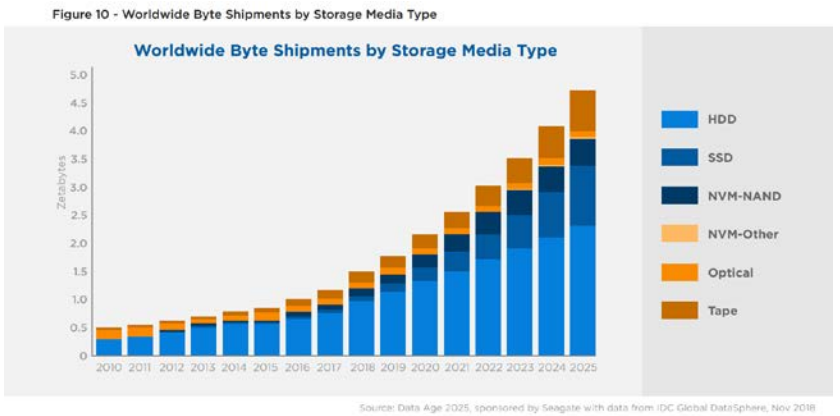
PDF/SOLUTIONS™

Memory Driver: Data Volume + New Computing Architectures

Flash Storage	Persistent memories	In-Memory Compute	Embedded Memories
o **3D NAND** o Cost/Bit scaling – Channel Hole Density – Vertical Scaling – Bits/Cell Increase	o **X-Point Memories** o Power/Speed scaling o Cost/Bit scaling – Min X-Y dimensions scaling – Multi-layer 3D-stacking	o **Low-Power, Low-Latency embedded NVM** o Multi-level, Analog Programming o Power/speed scaling o Cost reduction	o **Low-Power, Low-Cost code, data storage for microcontrollers, IoT** o Cost reduction o Reliability improvement o Power reduction
NEEDS: - **Fast Node transition** - High Yield - Innovation	- 3D-stacking - Fast Node transition - **High Yield**	- **Fast development and co-integration with Logic** - Performance/Yield - Cost reduction	- Fast development and co-integration with Logic - **Reliability/Yield** - Cost reduction



Source: Yole, MRAM Developer Day, Flash Memory Summit 2019



Key Takeaways

Reliability

- Safety, quality, and uptime are of paramount importance for new systems
- New chip technologies demand new sources of data to ensure reliability
- "Yesterday's yield problem is tomorrow's reliability problem"

Efficiency

- Rapid learning cycles are essential to creating a quality product
- Massive data collection is necessary to properly characterize reliability
- Quick, efficient data collection maximizes impact

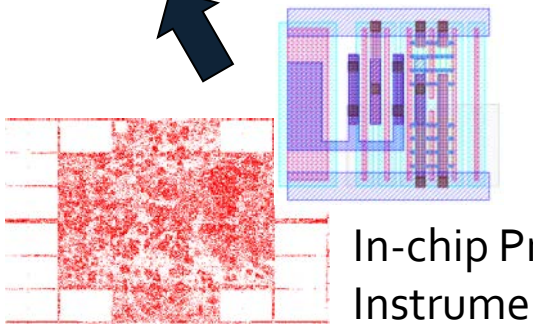
Foresight

- Closing the loop "from fab to field" enables predictive models
- New, optimized and efficient operational flows are made possible with AI

PDF Differentiated Data for Reliability, Efficiency, and Foresight

Design-for-Inspection™ System

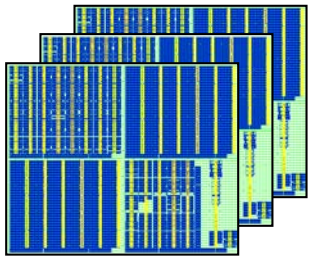
2nd generation
eProbe® 250
E-Beam HW



In-chip Product
Instruments

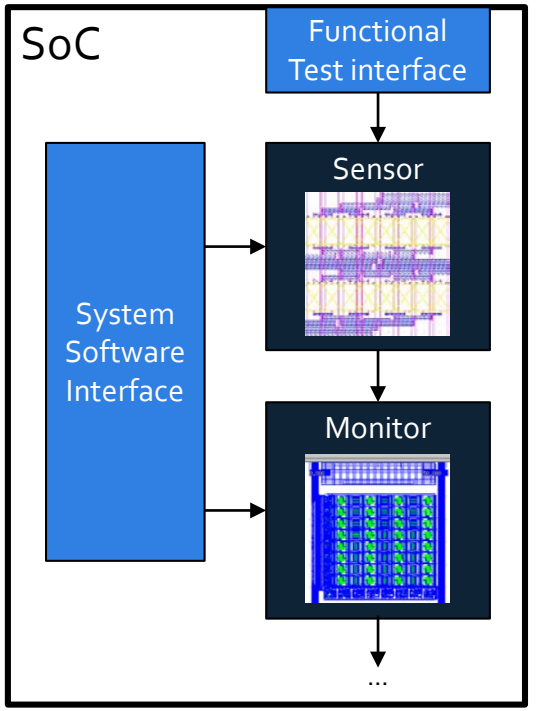
Characterization Vehicle® System

5th generation
pdFasTest®
E-Test HW



PDF CV®
Test Chips

CV® Core System



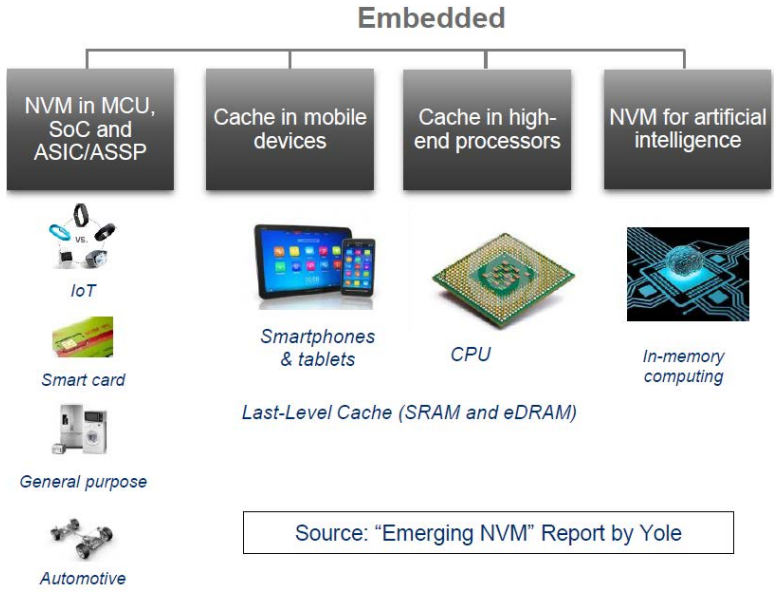
Inline

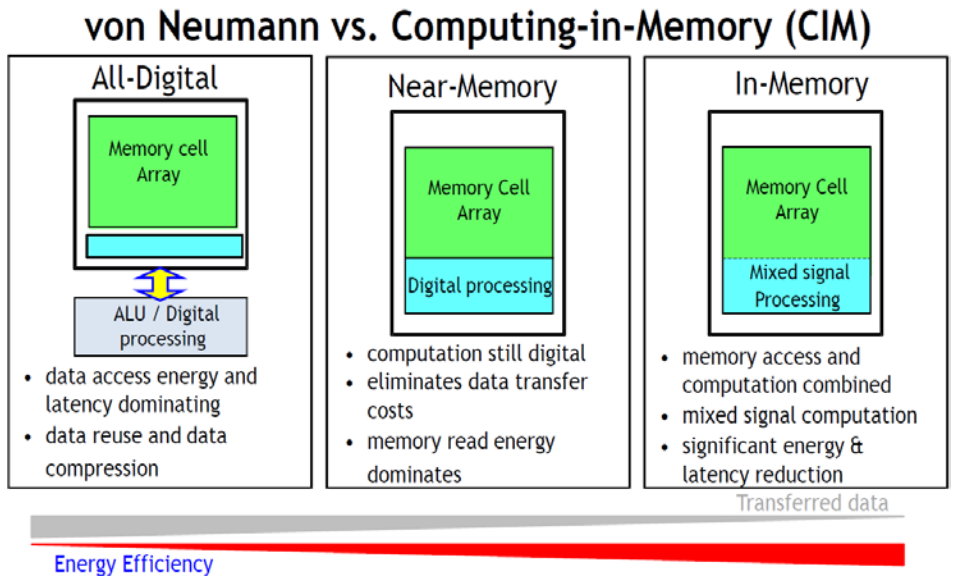
In-field

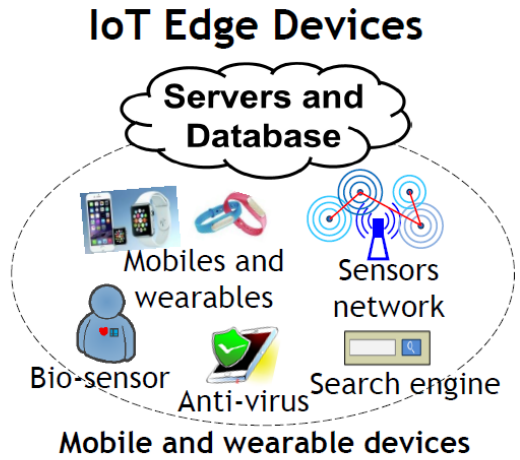
End-of-Line

Emerging Memories

- 62.7% of the total system energy is spent on Data movement† → **In-Memory Computing**
- Low latency Low-Power memory replacement SRAM → **MRAM for L3 Cache?**
- Emerging memories for Deep Learning → **On-chip High Density, Low Power solutions needed**
- Embedded memories for Automotive and IoT at 28nm and below → **Low power, High Reliability**



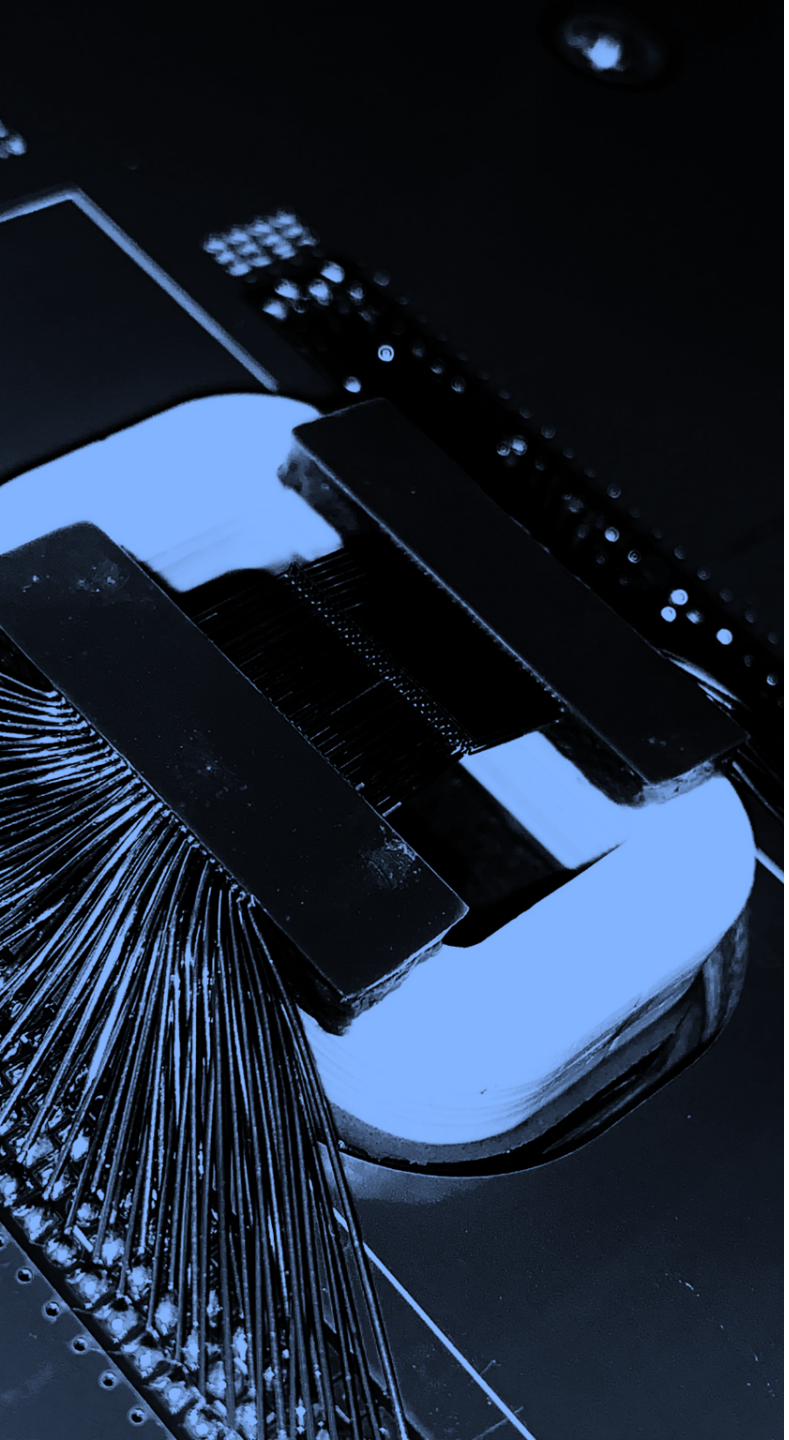




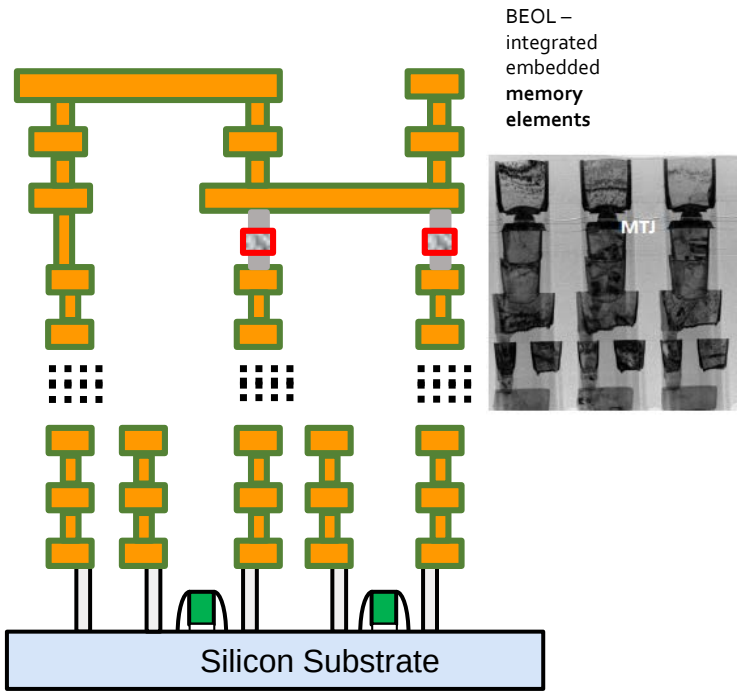
- Nonvolatile logics for frequent-off + instant-on devices

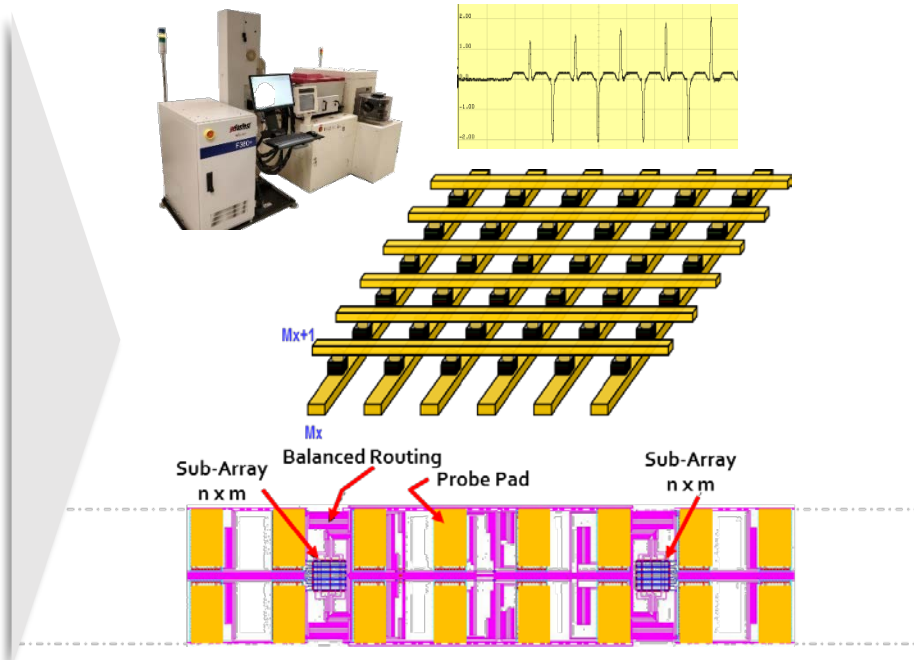
Source: VLSI Symposium on Circuits and Technology, Short Course, 2019

† Google at ASPLOS18



Enabling Emerging Memory Development



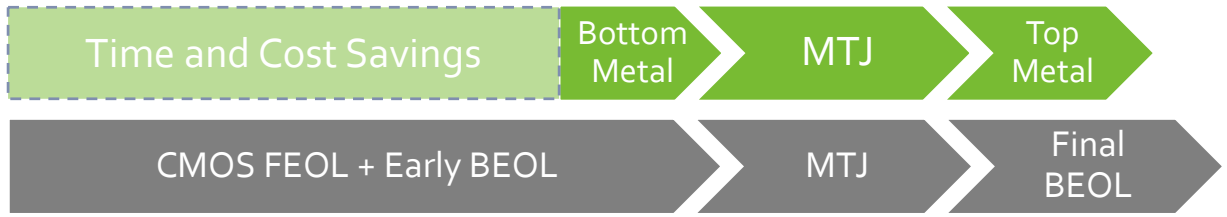


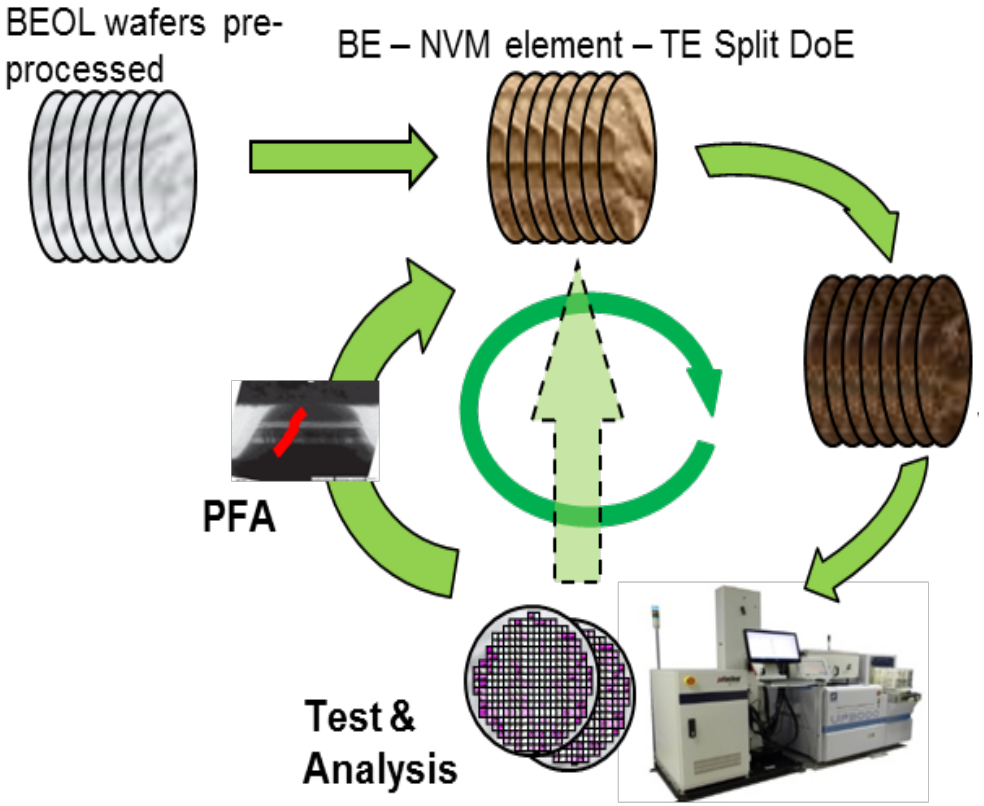
Full flow lots fabricate both back-end memory element and front-end selector devices → slow

Cross-point array with pdFasTest® parallel parametric pulse testing enables *efficient* learning

PDF Characterization System for Emerging Embedded Memories

- Unique Platform for BEOL-integrated Emerging Memories → MRAM, PCM, ReRAM
  - Innovative test structure and test method
  - Cross Point Array for high Bit statistics
  - pdFasTest® F380+ highly parallel pulsed parametric test
- Characterize millions of bits, millions of cycles in just hours



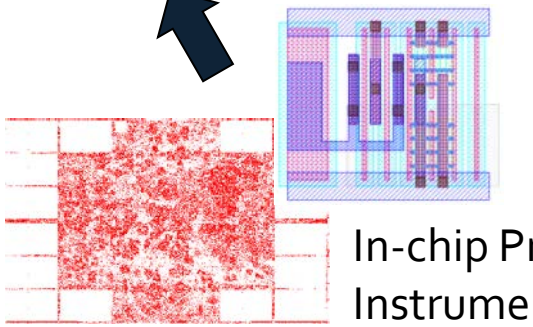


PDF's fast-learning characterization system *efficiently* enables the promise of emerging BEOL-embedded memories

PDF Differentiated Data for Reliability, Efficiency, and Foresight

Design-for-Inspection™ System

2nd generation
eProbe® 250
E-Beam HW



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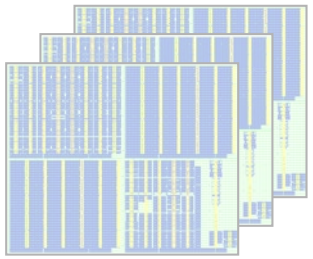
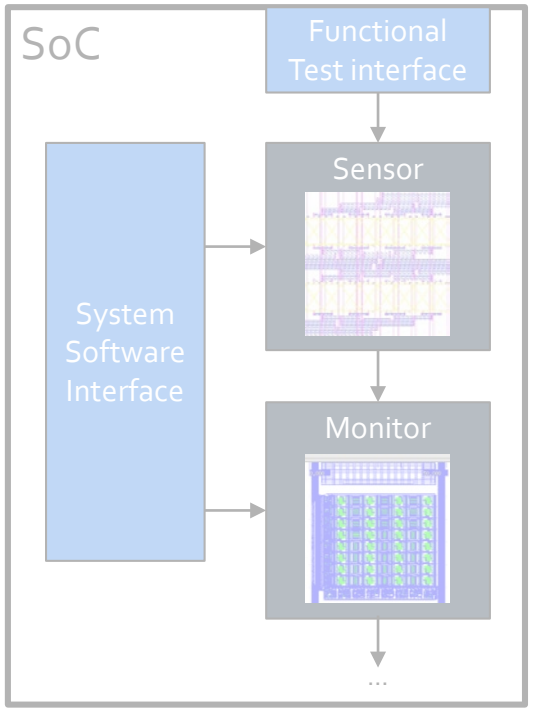


PDF CV®
Test Chips

CV® Core System

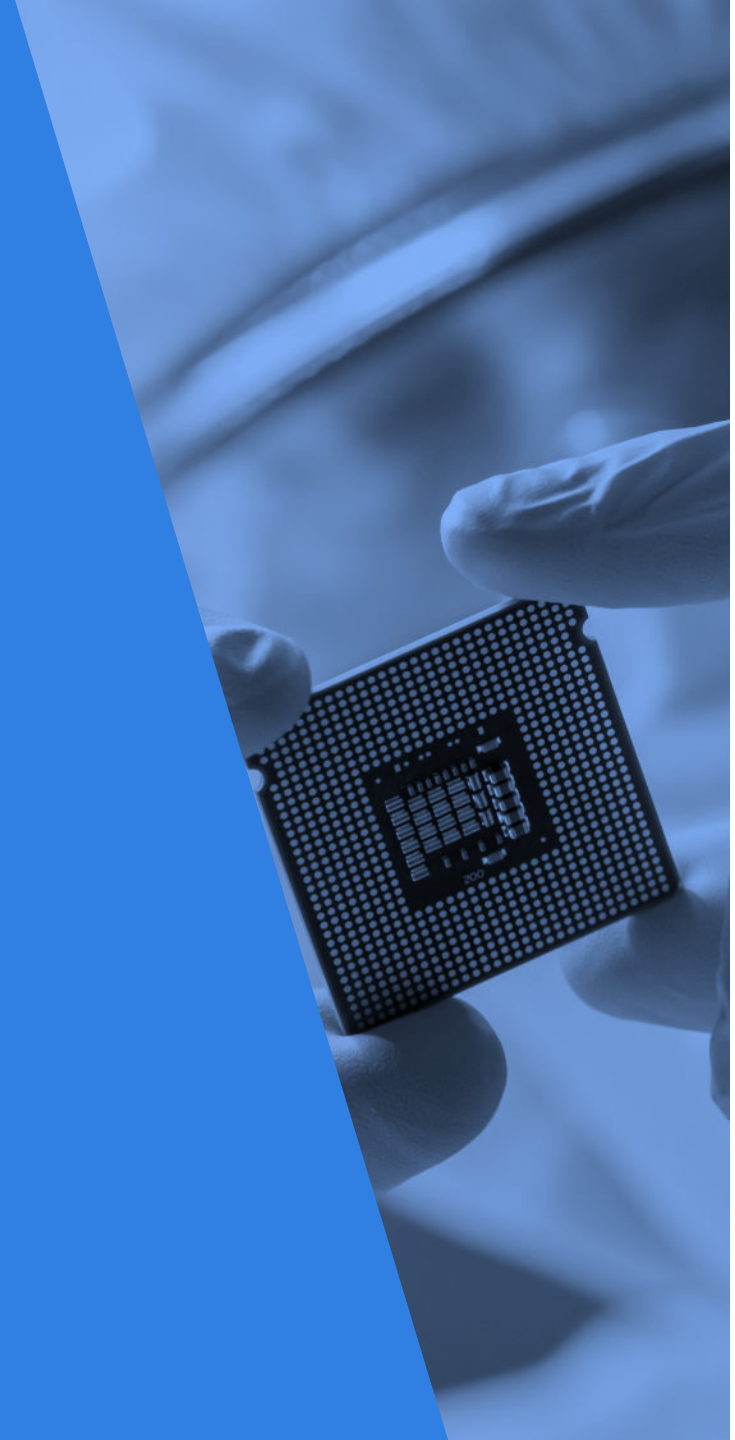


Inline

In-field

End-of-Line

Inputs from our Partners



- "Detect the Undetectable" → *Find electrically relevant defects buried inside 3D structures*
- "We are not late on a program because of functional yield, what kills us is we give the customer a chip, they package it, burn it in and figure out that there is a fundamental issue in a material stack or layout configuration. When that happens we lose 6 months to a year."
- "We need a non-contacting in-line solution for every wafer"
- "Can you measure every die in-line and predict reliability?" → *Reliability Grading*

The Advantages of the DFI™ System

DFI Capability

- DFI is a contactless electrical test measurement using an e-beam system
- DFI measurement speed (raw): 100M's DUTs/hr today, Billions of DUTs/hr next
- Calibrated Leakage Value: pA to nA baseline, capture outliers >10x

DFI Fill Cell

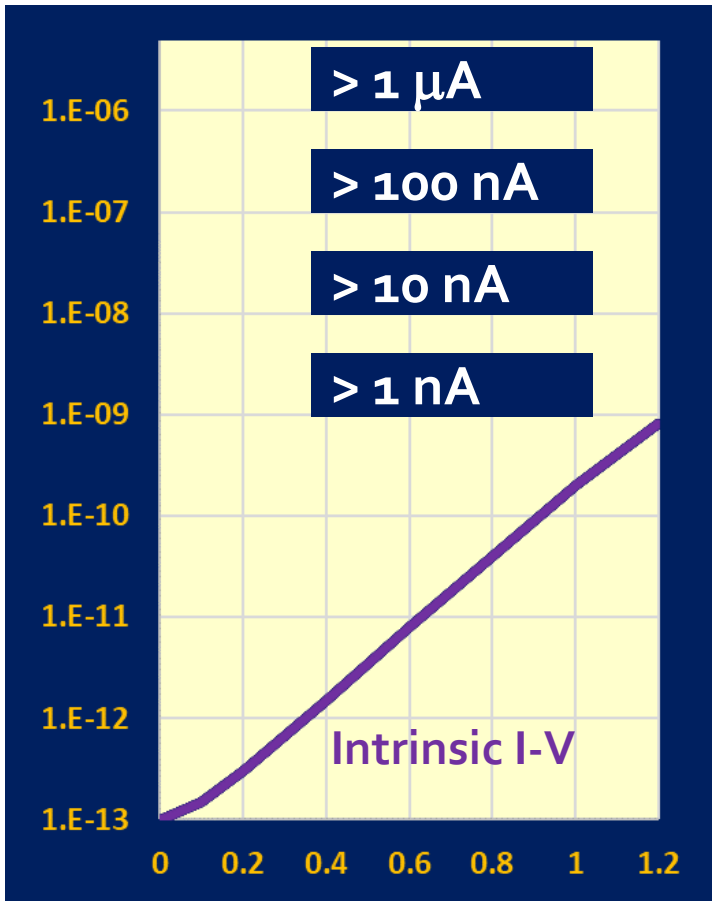
- DFI DUT quantity: 1B to 100B/wafer using in-product DFI fill cells
- In-die Reliability monitor: Focused DUT Design with DOE variants
- Reliability grading: Wafer and Die-level

DFI Scribe

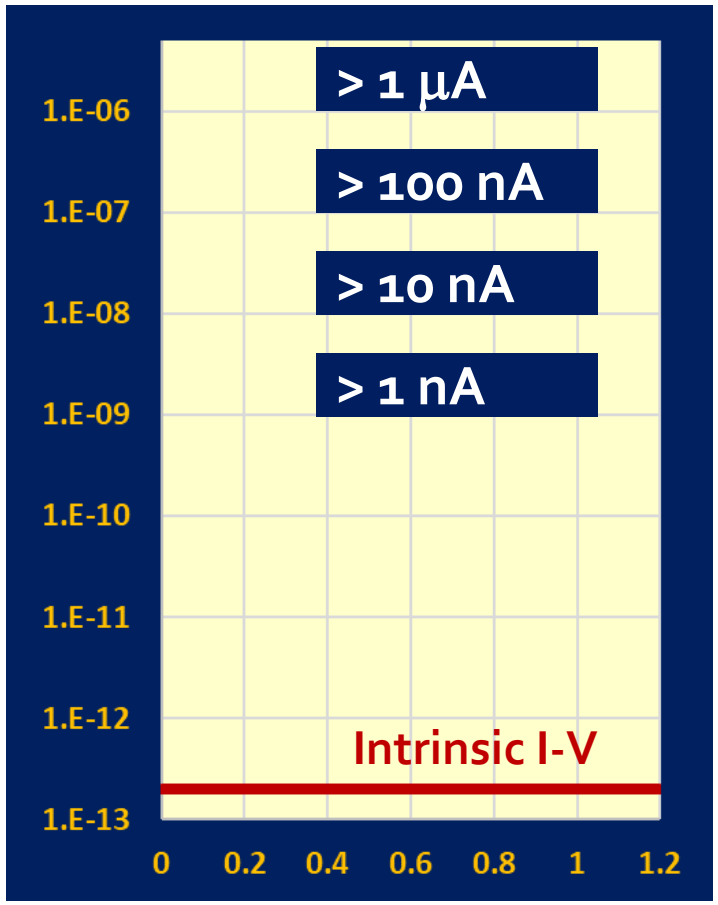
- DFI measurement density: 10-20M DUT's/mm2 (product-like environment)
- Yield metrology: Misalignment, Process window, Root-cause Detection, Hot-spot/Defect monitor

Why Does Leakage Matter?

Gate Dielectric



Spacer, Contact/Metal Isolation

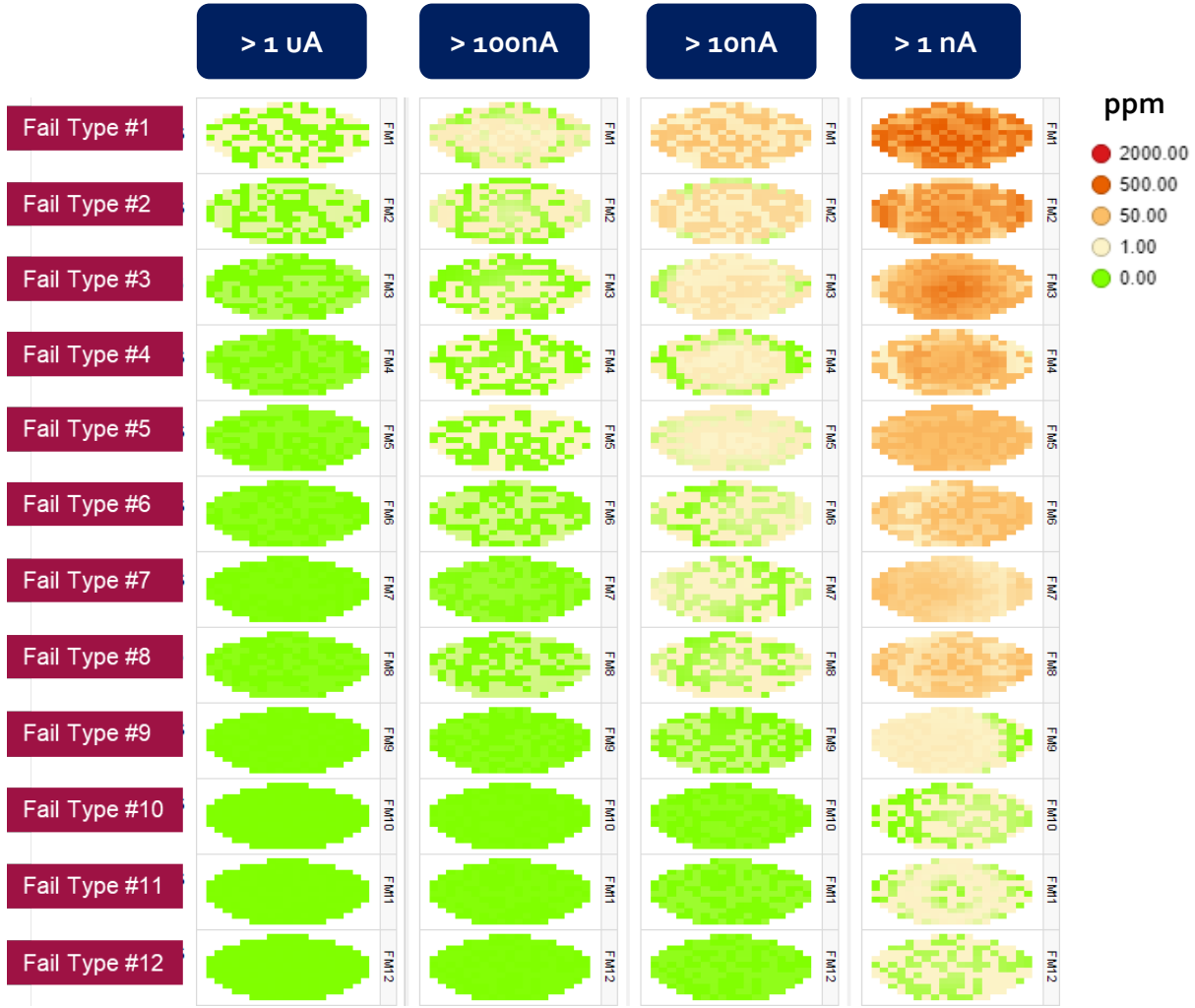


It is incredibly difficult to catch such tiny leakages in 10B's of transistors per chip

Leakage Outlier Bins
Identify Latent TDDB Weak Spots
RELIABILITY RISK

Typical Causes:
- Pinholes
- Dimensional Variation
- Process Damage
- Mechanical Stress

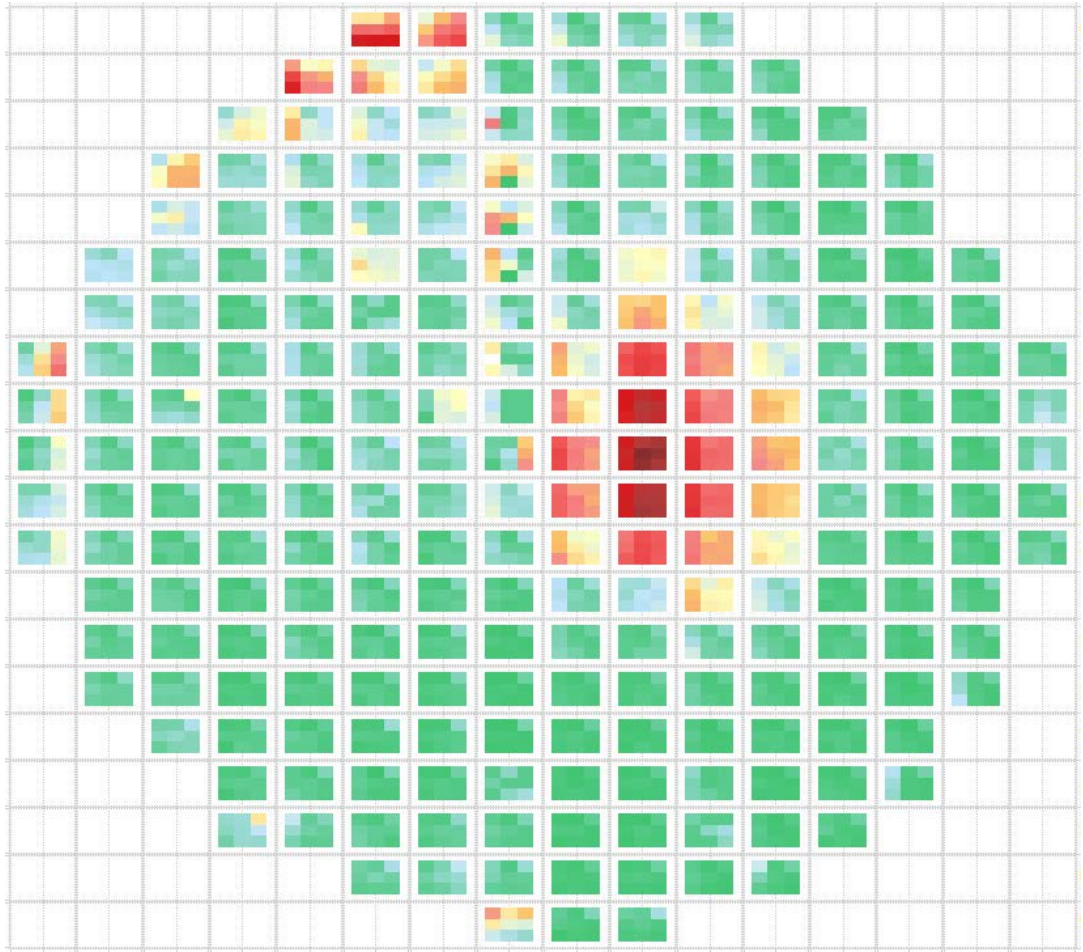
DFI™ Data: DUT Leakage Failure Rate Statistics



- Green die are zero ppm: Die with no failures observed
- Leakage level provides unique reliability insight into latent weak spots
- A composite of different fail mode estimates can indicate risk for early die failure or long term reliability

DFI *efficiently* scans billions of structures per wafer and catches tiny leakages at ppm to ppb levels, providing *early visibility* into potential *reliability risks*

DFI™ Die Control: Risk Grading



- High resolution map of every die for single fail type or composite of all fail types
- Spatial signature determines good/bad/risky die
- Within die perspective to assess risk for across field variability or local risk to certain fail type

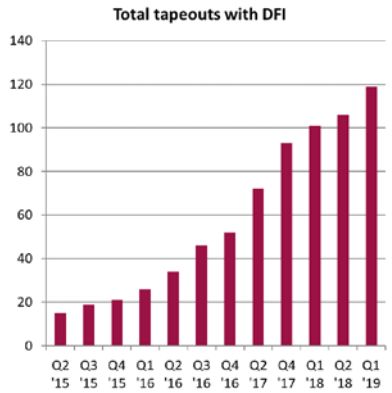
Detailed across-die measurement creates *foresight* and enables better risk screening per die than gross methods such as GDBN ("Good Die Bad Neighborhood")

What is DFI™ status today?

eProbe® System

- eProbe® 150: Running in full automation in 3 R&D fabs
- eProbe® 250: 1st tool running in full automation in production fab

Silicon



- Over 100 tape-outs to date, spanning 6 nodes
- ~60 Product/MPW tape-outs with DFI content

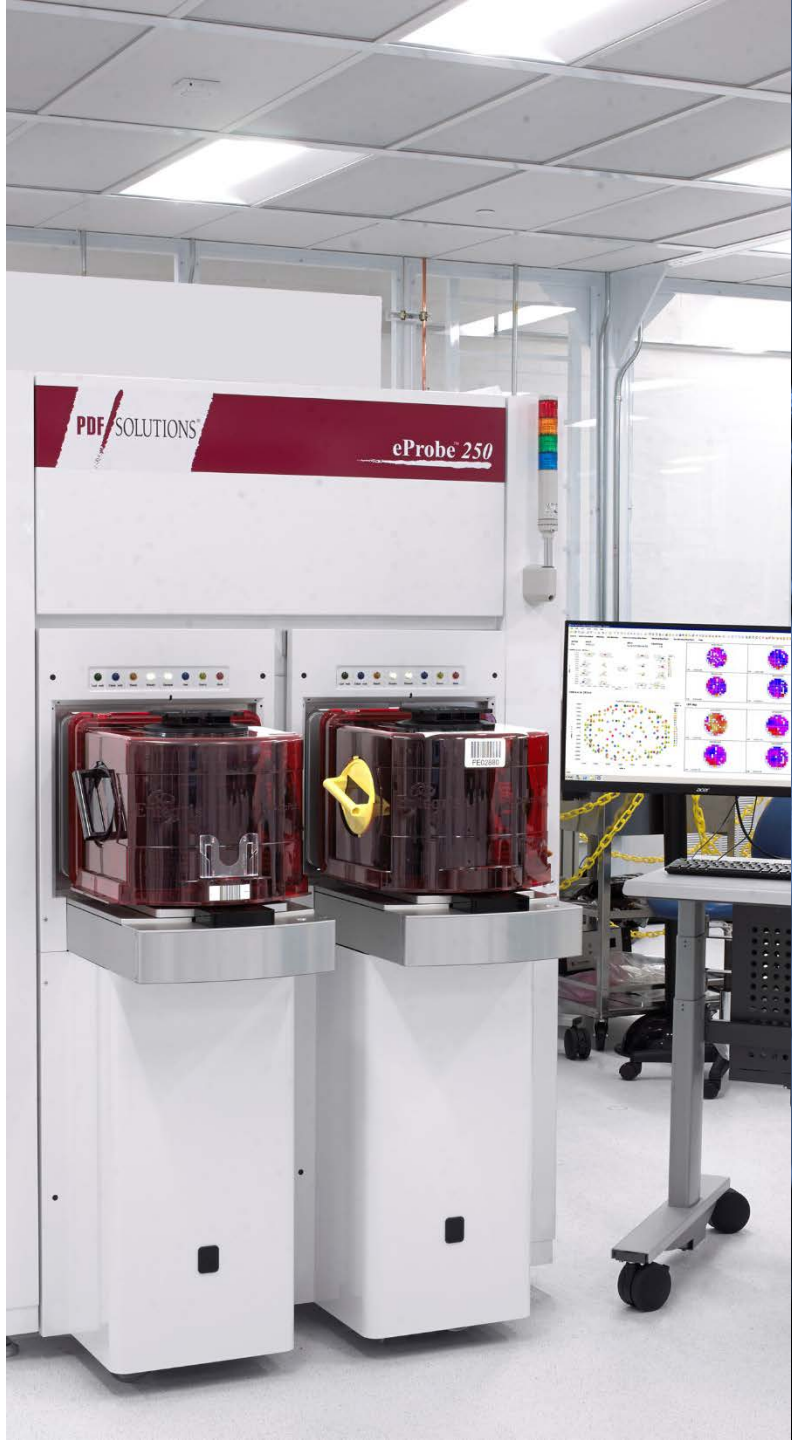
DFI™ Accomplishments 2019

eProbe® 150

- eProbe® 150 and Exensio DFI deployed at multiple sites using dense DFI test chips with throughput 10M's cells/hr
- In active use for yield learning on multiple nodes (22nm, 14nm, 7nm, 5nm)

eProbe® 250

- Demonstrated fill cell measurement throughput at 500M Cells/Hr
- Achieved first install in production fab complete with full automation
- Deployed for both scribe app and filler cell app at 7nm, 5nm in progress
- Demonstrated calibrated contactless leakage monitoring at DUT level
- Demonstrated applications for 3D NAND



Plenty of Work Remains!

- Demonstrate production-worthy wafer level and die-level reliability grading app by leakage monitoring of critical fail modes
- Make DFI™ an essential element for fab control by providing insight into otherwise undetectable issues
- Expand applications of DFI™ into 3D NAND & other non-logic technology

PDF Differentiated Data for Reliability, Efficiency, and Foresight

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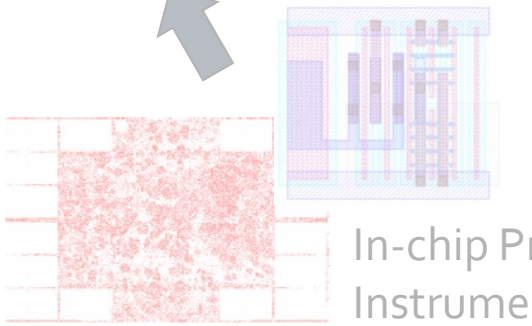

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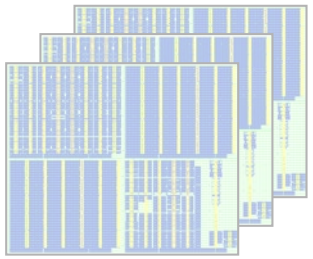
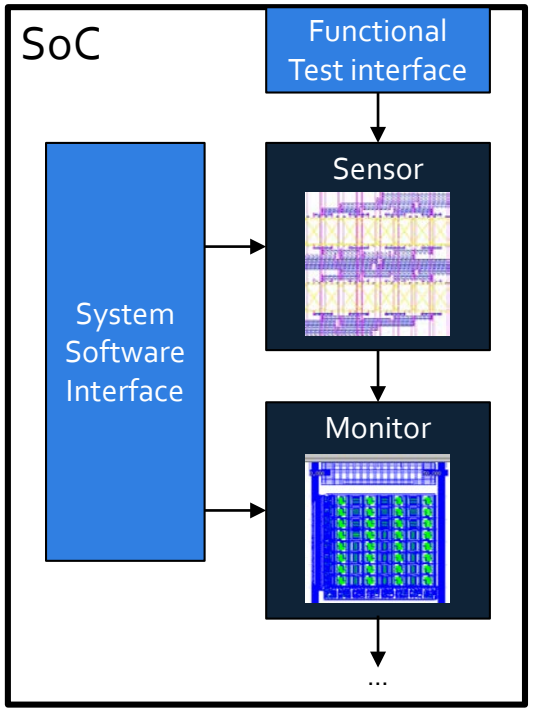


PDF CV®
Test Chips

CV® Core System

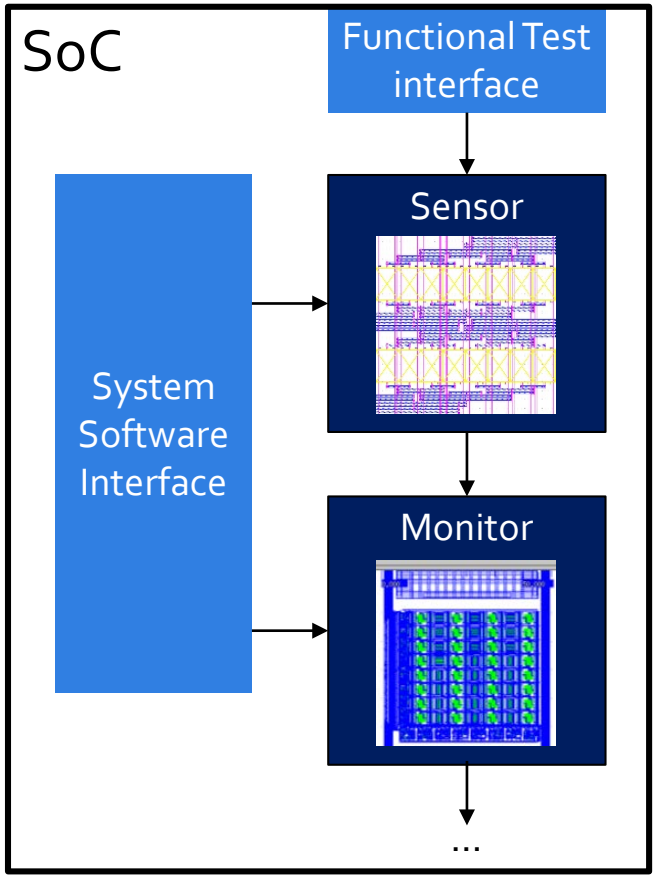


Inline

In-field

End-of-Line

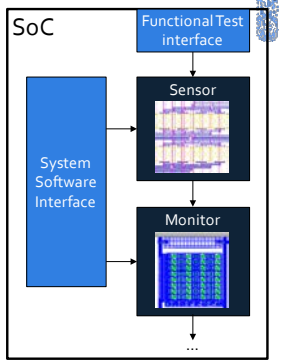
Leveraging IYR Technology: The CV® Core System



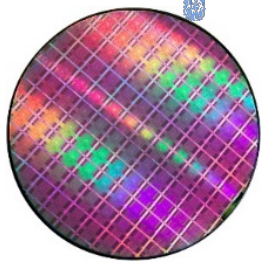
- The CV Core System integrates into your performance and reliability optimization strategy:
  - Capture weak die at t=0
  - Monitor Degradation in the field
  - Detect Change/Failure, Self Diagnosis, Failure Prediction
- PDF CV Core IP blocks are integrated using standard IP flows
  - GDS hard macro, LVS netlist, Verilog functional model, I/O spec
- The CV Core System enables:
  - Efficient t=0 reliability and performance screening
  - Mission mode t>0 reliability, performance monitoring, optimization
  - Seamless chip genealogy "From Fab to Field" for chip performance and reliability optimization across the complete product lifecycle

The CV® Core System

Exensio® Enterprise Analytics



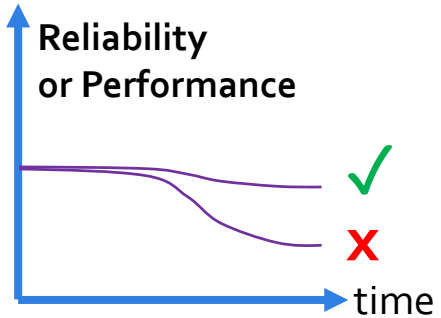
Chip/System Design

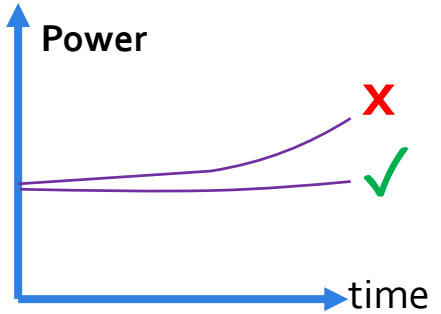


Wafer Manufacturing

Chip/Module/System Assembly and Test

Field Deployed Systems





Future | t < o | t = o | t > o

Optimize Next Chip Design

Feedback Key Issues to Manufacturing

Test Optimization
- Optimized flow
- Lower overall cost
- Improved Quality

Runtime optimization
- Longer reliability
- Power/Perf vs. Reliability
- Failure prediction

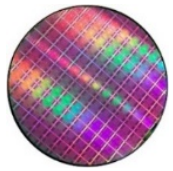
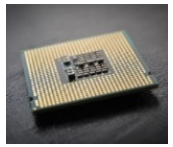
Value proposition ($$)

1. Greater reliability & predictive maintenance (uninterrupted service → $)
2. Product optimization (MWh → $)

PDF Differentiated Data Leverages Exensio® End-to-end Analytics

Inline | *E-Test* | *Wafer Sort* | *Final Test / Burn-in* | *In-System*




DFI™

CV® Core

CV® Infrastructure

- Product relevant electrical fail mode coverage, ppb resolution, across-field metrology
- Detailed and accurate parametric characterization
  - to ppm level in scribeline
- "Always available" characterization by SoC software at t>o
- Non-contacting inline process control enabled at Mo (t<o)
- t=o performance and reliability assessment
- Diagnose changes in performance and reliability after packaging
- Feed forward for predicted performance and test flow optimization
- Track system performance, reliability over time

Value Proposition

- Better Reliability (dppm, predictive fail)
- Lower cost ($$)
- Improved performance (speed, power)

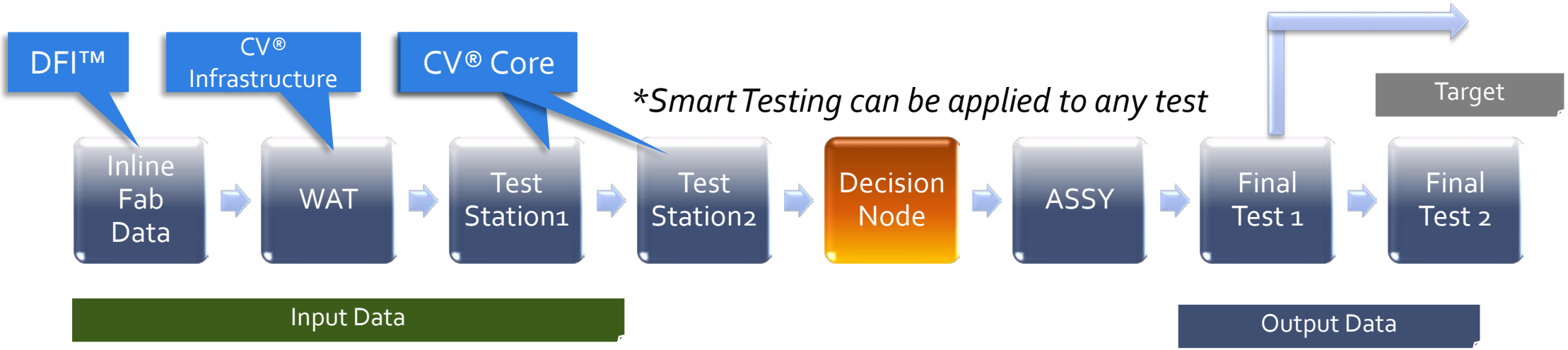
Front End Optimization+Control | *Back End Optimization+Control* | *In-Field Optimization+Control*

Exensio® Enterprise Analytics

Semantic model and AI-Enabled analytics

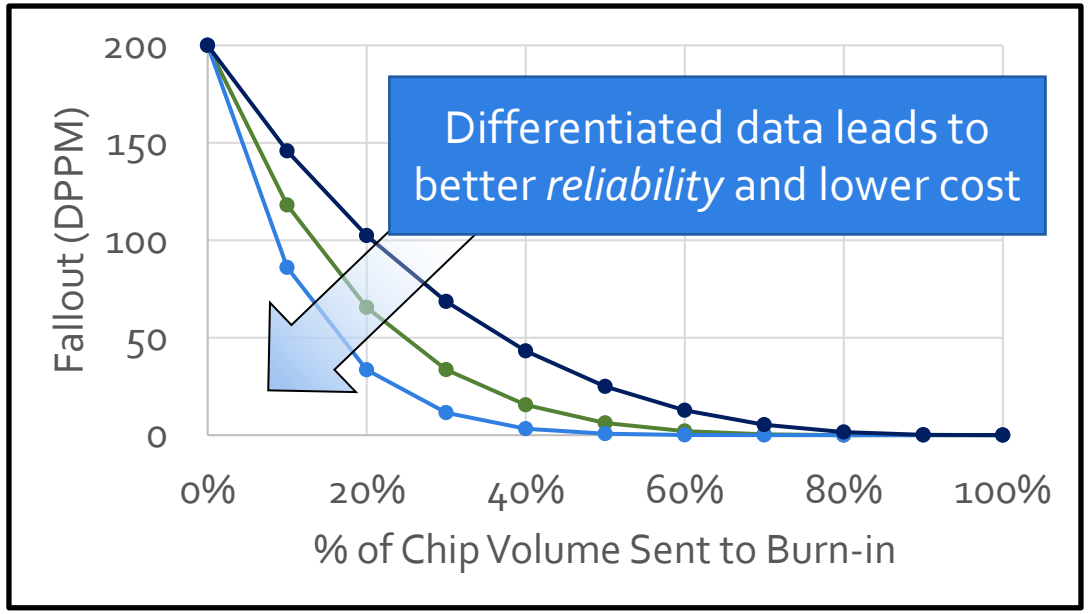
PDF/SOLUTIONS™

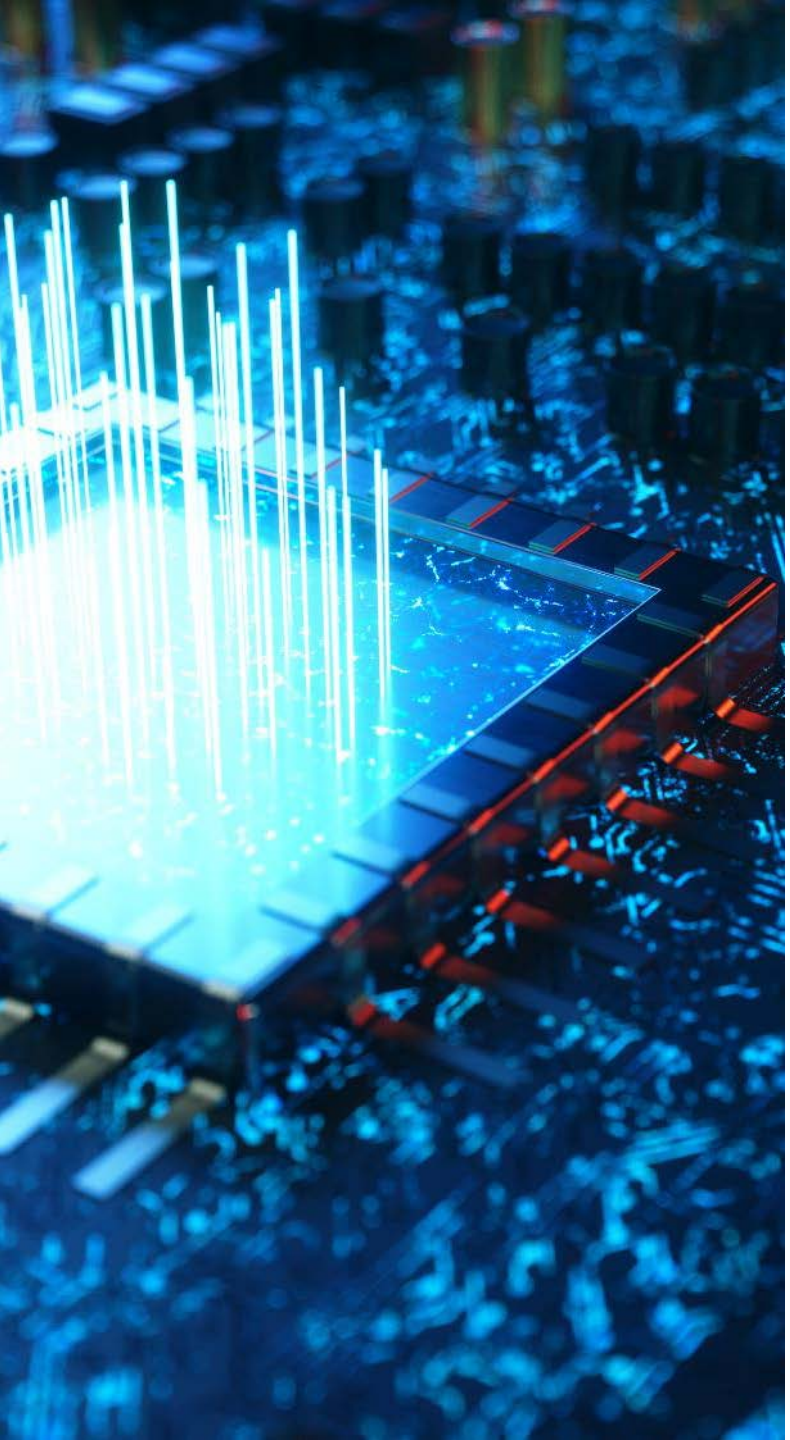
Smart Testing → Benefits from Differentiated Data



Goals:

- No risky chips to field, while diverting chips from expensive tests
- Improve quality and reliability by quickly identifying the root cause of field returns
- Focus test resources on product that are at the highest risk for failure
- Reduce test cost by diverting low-risk product volume away from expensive tests
- Smarter product binning by quality





Summary

- PDF's business has always been based on data
- Semiconductor system complexity continues to increase
- We continue to innovate new sources of data to efficiently improve reliability, performance, and yield, and reduce cost
- The Exensio® end-to-end analytics platform leverages this data to create *foresight* and optimize operational flows

Thank You

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