PDF/SOLUTIONS™

POSTED: OCT2020

Position Title: Process Design Engineer JC: 092000070

Position Location: Taipei, Taiwan

Relocation: Not Available

Travel Req: up to 50% to Customer Sites

PDF Solutions, Inc. (NASDAQ: PDFS) is a leading provider of yield improvement technologies, services, systems and analytics for the IC manufacturing process life cycle. Headquartered in San Jose, Calif., PDF Solutions operates worldwide with additional offices in China, Europe, Japan, Korea and Taiwan.

Position Summary: PDF is seeking an experienced Design Engineer to join the DFI team, to help define the Design For Inspection®IP. The Design Engineer will need extensive hands on experience in understanding and recreating fail modes and Root Cause Issues along with building VCI layouts.

Responsibilities:

- Understand target process fail modes and root causes and be able to probe client/team for information required to simulate the fail mode.
- Understand and comprehend design rules. Using design rules to make test structures robust vs. unwanted fail modes and be able to make educated decisions on which rules can be violated and which cannot
- Invent creative solutions to work around design rule limitation.
- Build Design-of-Experiments (DOE) for VCi cell designs.
- Plan DOE from design perspective (what is possible in design space)
- Build VCi cell layouts, while making cell designs which isolate the target fail mode and are as robust as possible
- Modify bit cells to make test structures able to detect target fail mode.
- Verify cells and fix DRC, LVS and ERC issues.
- Provide feedback on tool performance and create specs to improve efficiency and quality on our VCi design.

Qualifications and Skills

- Master's degree or higher in Engineering or related field
- Familiarity with semiconductor processing and key fail modes for 28nm, 20nm, 14nm, and/or 10nm technologies
- Familiarity with design rules and understanding the link between design rules and process issues

CV Design Engineer

- Familiarity with yield-related test structures like via chains, snakes, combs and testing techniques for these test structures
- Experience navigating semiconductor designs using basic CAD tools (Calibre, Cadence etc.)
- Experience using the UNIX operating system
- Excellent written and oral communication skills
- Excellent time and project management skills
- Highly professional, self-motivated and self-managed

Preferred Skills/Experience

- Experience using PDF's CV design environment (REC, blender,runbatch, etc.) -A PLUS
- Experience using DRC and LVS verification tools -A Plus
- Familiarity with standard cell designs to help create product-like test structures
- Experience with SRAM bit cells, esp. how to modify bitcell to make a test structure which is still relevant to detecting the target failmode
- Experience with voltage contrast measurement tools