PDF/SOLUTIONS™

Position Title: TC Consultant

Position Location: Santa Clara, California

Relocation: Not Available

Travel Req: up to 50% to Customer Sites

PDF Solutions, Inc. (NASDAQ: PDFS) is a leading provider of yield improvement technologies, services, systems and analytics for the IC manufacturing process life cycle. Headquartered in San Jose, Calif., PDF Solutions operates worldwide with additional offices in China, Europe, Japan, Korea and Taiwan.

Position Summary: PDF is seeking an experienced Consultant to join the Yield Improvement team, to serve serves as the primary contact for end-users of the Product. The Consultant will work on a team consisting of PDF and client engineers to identify and solve the performance and yield problems of advanced process. The candidate must have previous proven succesful experience with continuous interaction with clients at both the engineering and management level.

Responsibilities:

- Identification, diagnosis, and correction of characteristics of the FEOL or BEOL process or layout which limit product yield and/or performance.
- Design of experiments for FEOL or BEOL process module improvements.
- Statistical analysis of manufacturing data and simulation.
    - Projects are focused on leading edge semiconductor products and processes.
    - The work is focused on specific problems and must be performed in a timely and efficient manner.
- Drive value with customers by helping them identify and solve yield problems, analyze data.
- Assist customers in the creation of analyses and reports using Exensio®.
- Build and execute project plans for all of the above activities.
- Continuous interaction with clients at both the engineering and management level.

Consultant Qualifications

Qualifications and Skills

- Master's degree or higher in Engineering, Physics, or Micro-Electronics
- Experience in integration modules including STI isolation, gate, spacer, salicide and stress engineering; or process modules used in BEOL process including deposition, lithography, etch and CMP technologies.
- Experience and sound understanding of the modules used in the front-end of the line (FEOL) process including implantation, diffusion, photolithography, etch, and CMP modules; and /or multi-level interconnect and advanced dielectrics.
- Sound understanding of MOSFET device physics.
- Firm grasp on sequence and purpose of typical CMOS semiconductor manufacturing processing steps.
- Experience in determining design rule specifications.
- Experience using statistical data analysis techniques (t-test, linear regression, ANOVA) and statistical analysis software tools (Splus, SAS, RS1, JMP, Matlab).
- Experience using design of experiment (DOE).
- Strong semiconductor Yield, Product, Process or Defect Engineering background.
- Proficient in Microsoft Suite
- Excellent oral and written communications skills
- Highly professional, self-motivated and self-managed individual

Preference given to Candidates with the following Qualifications:

- Experience with modern (65nm, 45nm, 32nm or beyond) process integration issues.
- Sound understanding of product testing and analysis methods (logic function test, SRAM/ DRAM memory test, frequency/speed test, BIST, etc.)
- Sound understanding of low-k dielectrics, Cu dual damascene, Cu CMP
- Sound understanding of failure analysis techniques and good judgment concerning best application of such techniques.
- Experience with TCAD software, including process and device simulation.
- Experience with EDA software.
- Experience with PC and UNIX and the ability to write small scripts.
- IDM, Foundry or Fabless company experience.
- Knowledge of specific product categories such as SOC, DRAM or FLASH.