Advanced High Throughput e-Beam Inspection with DirectScan

Marcin Strojwas[a] Motosuke Miyoshi[b] Indranil De [a] Michael Keleher [a]

[a)]PDF Solutions, Inc.
[b)]PDF Solutions and Tokyo University

Abstract: Optical inspection cannot resolve critical defects at advanced nodes and cannot detect subsurface defects. Especially at 7nm and below, many yield and reliability killer defects are the result of interactions between lithography, etch, and fill. These defects often will have part per billion (PPB) level fail rates. Conventional e-Beam tools lack the throughput to measure PPB level fail rates. A solution is required with several orders of magnitude higher throughput than conventional e-Beam tools without sacrificing the ability to measure sub-20nm feature sizes. PDF has developed the DirectScan technology to scan billions of patterns of interest per hour. This DirectScan technology is an eBeam inspection technology that is designed and optimized to scan random product layout patterns. Using sophisticated product layout analyses, scanning recipes are created to drive the tool time of DirectScan technology to focus upon measuring relevant, voltage contrast observable layout shapes. PDF has deployed this tool on nodes ranging from 28nm down to 4nm products for at layer full wafer inspection within 24 hours or proportional sampling within 2 and 4 hour queue time limits. The results have enabled quantifying PPB fail rates per layout pattern in product die, identifying wafer spatial systematics associated with pattern fails, and detecting leakage currents corresponding to reliability risks.

Keywords: Design For Inspection, Voltage Contrast, Direct Scan, New Product Introduction, Process Control

1. Introduction

Shortfalls in actual yield achieved relative to entitlement yield are due to layout systematics and production variability. Entitlement yield is defined as the yield that a product should achieve if the only source of yield loss were random defects. The nature of layout systematics has changed at advanced nodes. Many of the most impactful layout systematics at advanced nodes are 3D – the resultant defects reside below the surface of the wafer. For example, MOL shorts such as contact or finfet to gate shorts are not visible at any time during the manufacturing process at the surface of the wafer. Similarly, via opens which frequently result from the interaction of lithography, etch, and fill processes lead to buried via voids which are also invisible at the surface of the wafer.

Yield learning cycles involve detecting an issue, quantifying its impact, diagnosing the root cause, implementing a corrective measure, and validating the corrective measure. Yield learning cycles that rely upon full wafer processing and end of line testing are inherently slow – often measured in cycle times of several quarters. Furthermore, end of line testing confounds all systematic and random yield loss sources, thereby making it difficult to assess the impact of a specific (non-random) yield issue. The ability to detect and characterize PPB level yield loss issues inline is crucial to overcome this yield learning cycle bottleneck.

In this paper, we report an advanced eBeam tool (eProbe 250) and system (DFI) that has been built and deployed by PDF to address these critical needs. We begin by reviewing two applications of this system – DirectScan and DFI Fill Cell Inspection. Subsequently, we summarize the hardware and system elements that enabled us to overcome technical challenges.

2. DirectScan

2.1. DirectScan Application Overview

The goal of the DirectScan application is to inspect a given layer of a product to detect yield and reliability relevant defects. The eProbe 250 has successfully measured layers with feature sizes as small as 1x metal layers in technology nodes as small as 4nm.

The DirectScan work flow consists of four stages as depicted in Figure 1. The first step is to identify a fail mode or set of fail modes of interest. This step dictates the layer at which the given wafer will be measured. The second step consists of analyzing the product layout and generating the measurement recipe. PDF's FIRE software is used to analyze the product layout. This software

identifies electrically relevant layout patterns for the selected fail modes. This tool also computes the expected polarity for the resultant layout objects. The next step is the actual measurement of the wafer on the eProbe 250. These measurements are now being performed on eProbe 250 machines that are installed in advanced fabs as well as PDF's lab. The final step is the analysis of the resultant data.

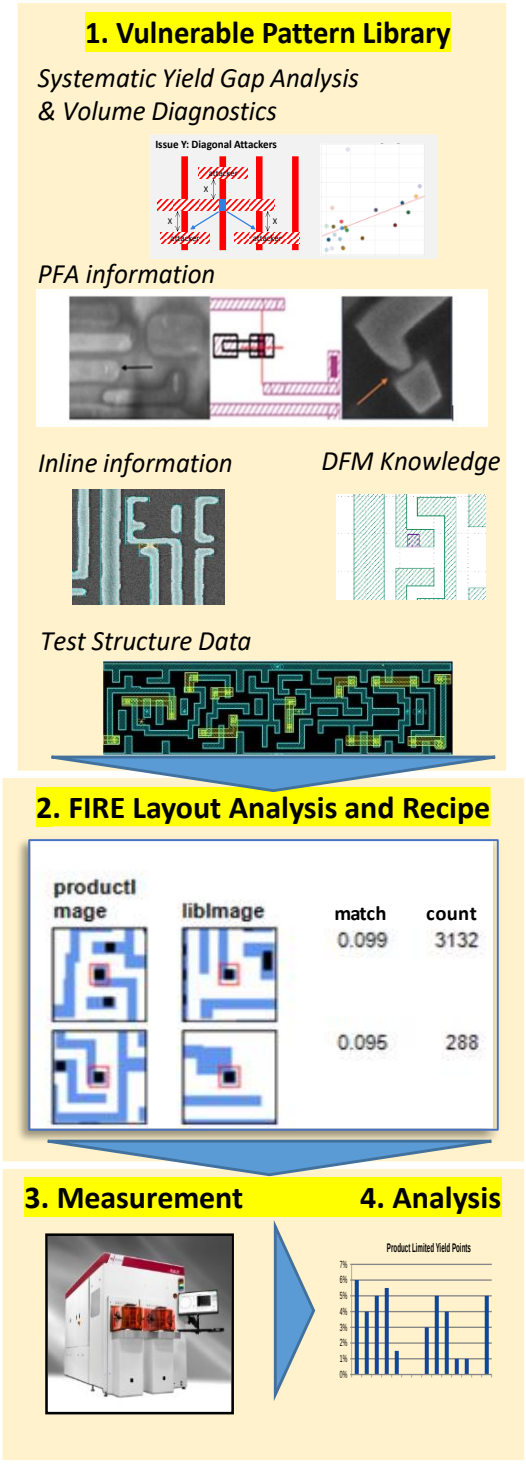

Fig. 1 DirectScan work flow.

Analyses have focused upon several key use cases including:

- Identifying which layout patterns are associated with systematic yield losses
- Quantifying fail rate per yield detractor
- Providing at layer A/B readouts for process and OPC splits
- Monitoring process health
- Accelerating NPI by detecting and diagnosing fails inline rather than at end of line test and scan diagnostics

2.2. DirectScan Application Example

DirectScan was used on a product being manufactured in 7nm technology. In this example, depicted below, DirectScan was used to identify high risk layout constructs in the products metal layers.

Over 20 billion instances of layout patterns were scanned at the selected metal layer using voltage contrast measurement. Dark defects were measured and recorded such as the defect shown in Figure 2.

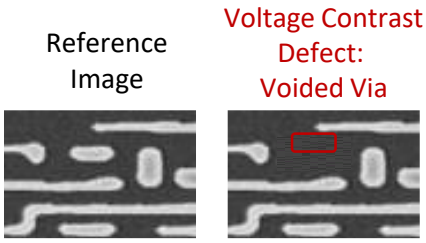

Fig. 2 Voltage contrast detected via void

The detected defects were summarized according to layout pattern family. Pattern families were formed using FIRE's automatic layout pattern classification engine. Total instances of patterns scanned per pattern family and fail counts were used to generate fail rates per layout pattern family. Fail rates were compared between a POR wafer and a wafer that received a split condition related to the layer and fail mode being measured as shown in Figure 3.

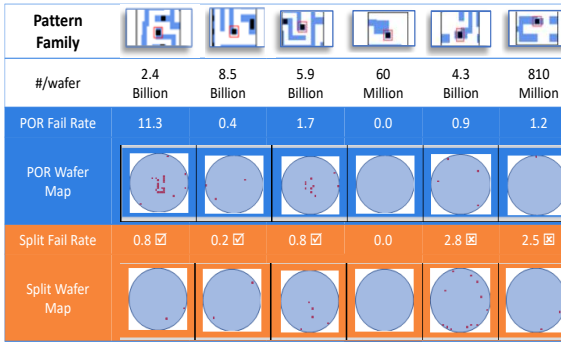

Fig. 3 DirectScan results comparing PPB level fail rate per layout pattern family across process split.

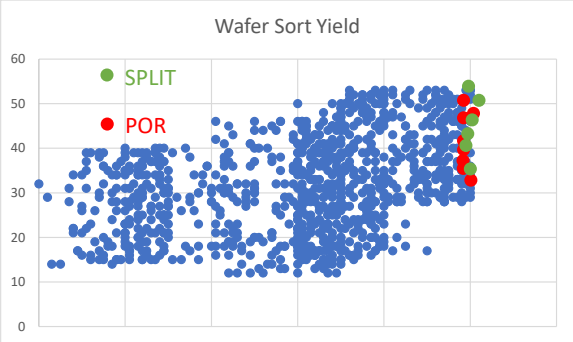

Fig. 4 Wafer Sort Yield of wafers in split lot measured by DirectScan.

The results revealed that in fact the process split significantly improved the fail rate of the previously problematic layout pattern families. Those fails typically occurred most frequently near the center of the wafer. However, the results also revealed that the new process condition resulted in an uptick in fails for other layout pattern families near the edge of the wafer.

Observing these changes required PPB level measurement capability. In the absence of this PPB level measurement capability, a foundry and their fabless customer would need to run multiple lots to end of line and then conduct product test. Simply running product lots to end of line would make it difficult to discern the impact of the process split, as is shown in Figure 4. The green dots represent the yield of wafers from the split lot with the split condition, while the red dots represent the yield of wafers from the split lot with the POR condition. The blue dots represent the yield of the wafers from prior lots during the past six months of production. As you can see, there is a significant overlap between the green and red dot populations. Also the variation in the yield of wafers is larger than the impact of the process split.

The split condition delivered an economic benefit of greater than 5% yield improvement. Significant additional benefit was gained because the split condition improved a reliability failure mechanism impacting partially voided vias. In the absence of DirectScan, many more split lots would need to be run to see the improvement result with statistically significant confidence. By running DirectScan, the impact was observable and quantifiable directly at the metal layer of interest while also providing insight into accompanying issues that needed to be addressed.

3. Design For Inspection (DFI)

3.1. DFI Application Overview

Most chips designed for advanced nodes consist of 5-15% empty space in the standard cell layers which we refer to as “white space”. This white space represents an opportunity to instruments chip designs with eBeam testable test structures which we refer to as “DFI Fill cells”. Within standard cell regions, these DFI Fill cells look similar to conventional fill cells except they are modified to be sensitive to a particular fail mode of interest and include a metal pattern that is optimized for high throughput measurement as shown in Figure 5.

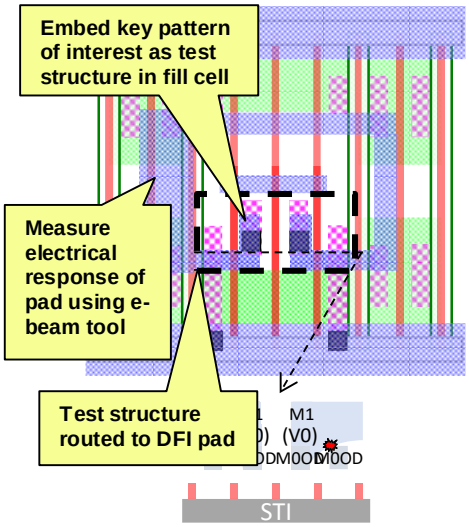

Fig. 5 An example of a DFI Fill cell.

Insertion of DFI Fill cells is transparent to existing design flows. DFI Fill cells are swapped in place of conventional fill cells. DFI Fill cells are selected to provide observability for critical fails modes. In addition to detecting shorts and opens, the DFI Fill cells excel at detecting leakages that represent soft shorts which often correspond to reliability weaknesses.

In addition to inserting DFI Fill cells in white space within logic blocks, DFI Fill cells can be inserted in the gaps between logic blocks which we refer to as “inter-block space”. These inter-block space regions tend to provide contiguous chunks of area that can be used for DFI Fill cells that require a larger footprint than what is compatible with white space.

Another critical insertion point for DFI Fill cells is within scribe lines. Although scribe lines represent a scarce amount of area, scribe lines may generally be used to insert DFI Fill cells with pushed design rules. The DFI Fill cells with pushed design rules enable two valuable sets of information: Firstly, they enable directly measuring process margins inline. Secondly, they enable calibrating gray scale leakage measurements from DFI Fill cells to electrical measurements that can be gained from scribe structures. An example of this application for reliability grading is provided in the next section.

3.2. DFI Application Example

Unintentional shorts in chips are a particular concern for reliability fallout and field failures. Soft shorts with minimal current flowing early in the lifetime of a chip can become catastrophic field failures over time. The minimal current that is flowing across a highly resistive filament will tend to cause heating and enable metals to further flow and create bridges between unrelated nets in a chip. Those bridges can cause field failures. During chip testing, the soft shorts may not be detected as failures because the nets are still driven to their correct values by stronger connections.

In the example shown in Figure 6, a set of DFI Fill cells were embedded in a 7nm product. The DFI Fill cells were designed to detect critical fail modes with an emphasis upon the FEOL and MOL. Dozens of fail modes were observable with these DFI Fill cells spanning across a DOE of layout configurations. A total of 105 Million DFI instances were embedded in the product logic area per die.

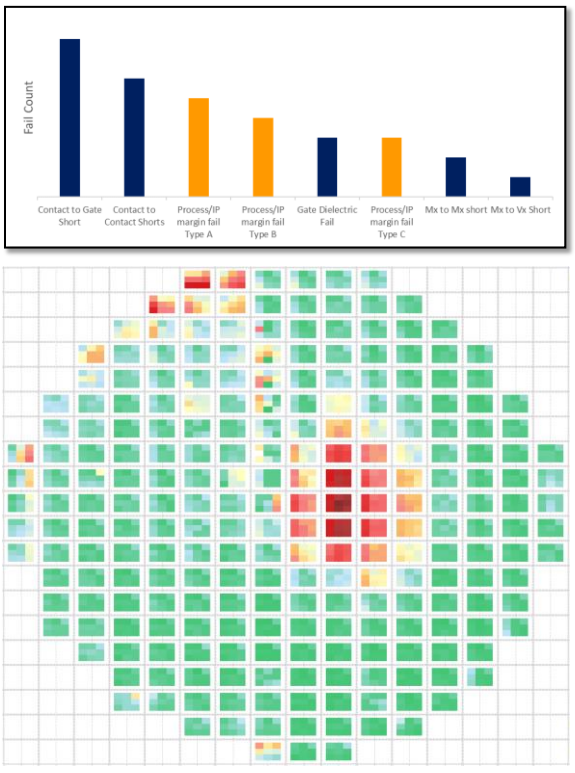

Fig. 6 Results of DFI Fill cell measurement.

Figure 6 shows the results of measuring the DFI Fill cells for a single wafer. The aggregate fail count

per fail mode is shown in the form of a pareto. Fail modes corresponding to shorts are shown in blue while fail modes shown in orange reflect opens. The wafer map provides a view of the distribution of the fails across the wafer and within each die.

Opens are detected when a DFI Fill cell pad for an open fail mode turns dark. When no defect is present the pad will be bright due to the secondary electrons emitted when a path to ground is present. Shorts are detected when a DFI Fill cell pad turns bright. The DFI system is able to measure "gray scale" levels corresponding to soft shorts or leakage currents – we refer to this as the DFI Electrical Response Index (ERI). In order to calibrate the gray scale levels to electrical leakage magnitudes, DFI test structures were placed in the scribe that enabled measuring electrical leakage and DFI ERI on the same test structure.

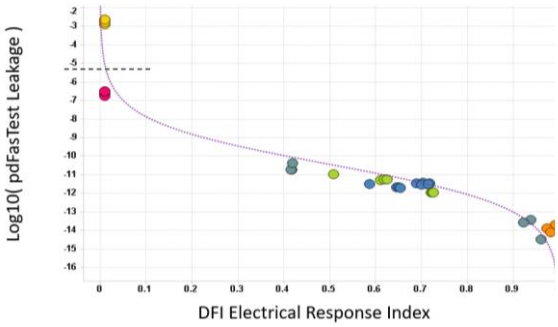

Fig. 7 Model relating electrically measured leakage current (y-axis) and voltage contrast measured DFI ERI (x-axis) from the same test structure in scribe.

The ability to translate DFI ERI measurements to electrical leakages enabled setting reliability specifications. Figure 8 shows the results of setting various thresholds for leakages for each fail mode.

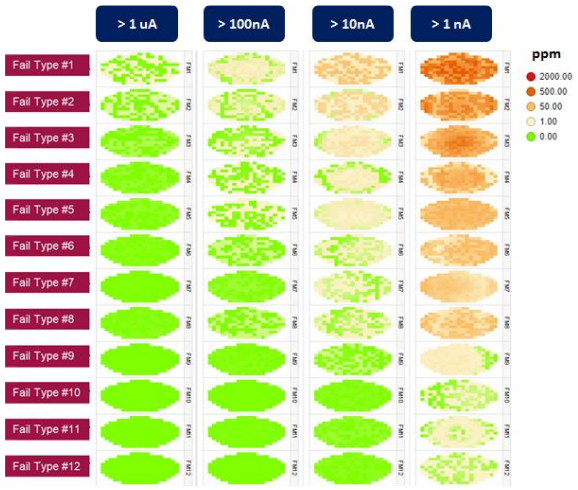

Fig. 8 DFI Fill cell fail rates measured with various leakage thresholds.

The fail rates and resulting wafer spatial signatures for the fail modes corresponded to the spatial signatures for the yield and reliability fail modes. These subtle levels of leakage currents will frequently escape product wafer sort test. By measuring the DFI Fill cells inline, these leakage currents can be captured and used for reliability grading applications.

4. eProbe 250 eBeam System

The applications discussed above were enabled by the throughput and resolution capabilities of the eProbe 250 eBeam system. The eProbe 250 eBeam system is designed, produced, and offered by PDF Solutions. The eProbe 250 system is tuned to perform voltage contrast measurements using vector scanning mode. By operating in vector scanning mode, the system is able to direct the eBeam measurement time to measuring locations in the wafer that actually matter. The embedded software in the eProbe 250 system performs realtime registration during measurement and employs an artificial intelligence based system for learning the relationship between layout and measured ERI on silicon.

The throughput of the eProbe 250 is dictated by the field of view (FOV) and the stage speed. For minimum feature dimensions at advanced nodes, a 45um x 45um FOV is used and a 20mm / sec stage speed. This results in a full wafer scan time of

approximately 22 hours. We refer to full wafer scans as running in “Discovery Mode”. Customers will typically use Discovery Mode when they would like to identify new or unknown failing patterns at a given layer.

The eProbe 250 is also used in “Production Mode” when queue time limitations dictate that scans must be limited to 2-4 hours. Customers will typically use Production Mode when they are investigating specific issues that may be more pronounced or certain regions of a wafer or otherwise intelligently sampled. Customers may also use Production Mode to split a full wafer scanning recipe across approximately 10 wafers. Thus they can achieve the same aggregate coverage as Discovery Mode while adhering to queue time limitations.

When use cases target measuring larger feature sizes, the eProbe 250 operates with a FOV of 45 um x 45 um and can travel at a stage speed up to 100 mm / sec. The resulting throughput enables full wafer scans within 4 hours for larger feature sizes.

The architecture of the eProbe 250 enables further throughput improvements that will be forthcoming during the next few years. Importantly, these throughput advances will be enabled by the vector scan capability of the system and the associated software system. Therefore throughput improvement will not come at the expense of sacrificing resolution by increasing pixel size as some raster scan machines do. The eProbe 250 architecture also provides a scalable trajectory for achieving throughput improvements in contrast to multi-beam eBeam systems which rely upon adding beams to achieve sublinear throughput scaling and super linear processing and storage cost increases.

5. Conclusion

The DirectScan and DFI applications are revolutionizing the best in class practices for inspecting sub-surface defects at PPB levels of statistical significance. These capabilities are enabled by the eProbe 250 hardware. The resulting system provides faster yield learning loops which are critical for the types of defects that are limiting yields at advanced nodes. The system also addresses the needs of high reliability products by enabling inline reliability grading.

The system has been deployed at multiple foundries across multiple products. Critical systematic yield loss sources have been discovered with DirectScan. These include yield loss sources that were previously unknown to the fabless and foundry customers.

DirectScan and the broader set of DFI applications have the opportunity to advance the state of the art in inline control, test, diagnostics, and FA. By integrating DirectScan and DFI data with test diagnostic data: the additional goal of earlier and more precise detection, identification, quantification, and classification of systematics can be achieved.