New Method for BEOL Overlay and Process Margin Characterization

[1]Linrong Yang, [1]Runling Li, [1]Jiadong Ren, [1]Linlin Sun, [1]Yawen Xue, [1]Wenchao Yang, [1]Ruilin Zhang, [1]Yefang Zhu, [1]Yan Zhang
[2]Ikai Hsu, [2]Haiqiong Zhang, [2]Guifeng Zhang, [2]Yingying Fu, [2]Shan Yin, [2]Yujie Jia, [2]Bo Yu, [2]Tomasz Brozek
[1]Huali Integrated Circuit Corporation, Shanghai, China
[2]PDF Solutions, Inc., Santa Clara, USA

Abstract

This paper presents a new method, Design-for-inspection (DFI) to characterize overlay. Using design-assisted voltage contrast measurement, the method enables in-line test and monitoring of process induced OVL and CD variation of back-end-of line (BEOL) features with litho-etch-litho-etch (LELE) patterning. While only some of the features of multi-color patterning scheme are chosen to be aligned directly, other combination of metal line and via colors may have uncontrolled misalignment risking open or short failures. The paper shows how the complete metrology coverage of multi-color combination between dual patterned Via and dual patterned Metal Lines helps driving the improvement of overlay and process margins in 14nm technology. The enlarged process margin for Via Opens will drive yield improvement and better reliability.

(Keywords: BEOL, LELE, Overlay, Process Margin, Design for Inspection, Voltage Contrast)

Introduction

Moore's Law demands Critical Dimensions (CD) scaling to support higher density of devices per chip. One of the consequences of interconnect scaling is moving to multi-patterning scheme for technologies below 20nm generation, until eUV becomes viable at 5nm node. Among two approaches – Spacer-Assisted Dual Patterning and Dual Exposure with LELE (Litho-Etch-Litho_Etch), the latter offers more flexibility, especially for bidirectional routing [1]. Also, it is the only choice for Via scaling, allowing to print closely spaced holes.

One of the challenges of multi-exposure patterning within the same layer is maintaining the tight control of the overlay (OVL) between all features of the layers above and the layers below, which depends on the patterning choices and on the implemented alignment scheme.

In-line metrology is adopted at patterning level ("After Develop" and "After Etch" metrology) to provide immediate feedback to manufacturing and enable a rework operation, if possible. Such metrology is very efficient to capture optical misalignment effects, but cannot ensure that the electrical response will also be the same. Wafer bowing and in-film stress may cause additional pattern shifts and cause Open/Short fails, even if initial optical overlay results showed no problem. We propose a new metrology approach, utilizing PDF Design-for-Inspection methodology to monitor the misalignment electrically in a non-contact way.

Design-for-Inspection™ (DFI) Metrology

The DFI methodology is based on the concept of a series of test structures, each having incrementally increasing built-in misalignment between two subsequent layers (e.g. Metal Line and Via). Misalignment spans the whole width of a feature, including extreme cases where the structure would electrically fail (Fig. 1).

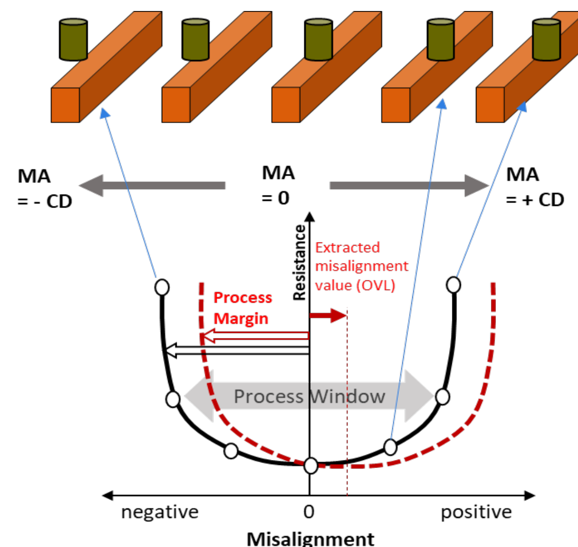

Fig. 1. Principle of electrical measurement of the misalignment vector (OVL – "overlay") using a set of test structures.

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Such structures can be used to characterize the overlay, process window and margin for all critical layers [2]. The U-shape Resistance plot in Fig.1 allows extraction of the misalignment vector and the process margin for failure-free patterning. In the case of DFI structures, Voltage Contrast (VC) gray level signal is used instead of the resistance. DFI structures offer an advantage of the density, sub-nm level resolution, and high-speed non-contact testing. PDF eProbe e-beam system is used to perform high speed VC data collection from large number of DFI cells embedded in the product layout and in the scribe lines between product dies.

DFI Overlay and Process Margin results

In this work we applied DFI methodology to monitor OVL in M1-V0 self-aligned Via process patterned with two LELE steps in 14nm FinFET technology. The alignment scheme and in-line metrology are shown in Fig.2, where M1/V0 A and B represent first and second LE pattern for M1 and V0, respectively.

M1A is set as anchor point for V0A and V0B Overlay, and is used for Advanced Process Control (APC) feedback and process monitoring. Quality of V0A-M1B and V0B-M1B OVL rely on the M1B, and althought monitored, was not used for APC. As a consequence, overal OVL performance may differ between V0 to M1A and V0 to M1B patterns. Fig.3 shows V0-M1 mean+3 sigma OVL inline wafer-level trending collected using DFI over a period of 2 months, where each color represents different V0-M1 color combination for OVL data acquisition.

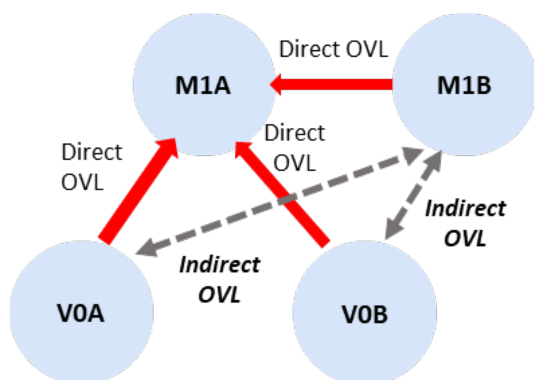

Fig. 2. Alignment scheme for dual exposure M1 and dual exposure Via0. M1B, V0A, and V0B are all directly aligned to M1A, while V0A and V0B overlay to M1B requires additional alignment control (they can be out of spec, even if all direct OVL vectors are within spec limits)

During initial data collection, V0A/B-M1B OVL is found to perform much worse than V0A/B-M1A OVL, with no clear OVL delta between V0A-M1 and V0B-M1, regardless of M1 exposure. By comparing OVL performance across 4 different V0-M1 color combinations, M1A-M1B is the top suspect to induce high OVL for downstream V0A-M1B and V0B-M1B. Although DFI is not measuring M1A-M1B OVL directly (due to design-rule limitation for test structure design), M1A-M1B OVL can be extracted from interpolation of V0-M1A and V0-M1B OVL values. Clearly, the OVL errors in the initial time period were above the specification limit and created high risk of yield loss due to potential V0-M1B open. Corrective actions were introduced by the engineering team for M1A-M1B overlay improvement. After optimizing lithography APC scheme and updating overlay models, significant improvement in V0-M1B OVL was achieved. This result is reflected in the OVL trend shown in later time period in Fig.3. OVL wafer maps for V0-M1 and extracted M1A-M1B pre- and post- improvement are shown in Fig.4. Larger marker size indicated larger OVL error, and the color shows the error sign - the polarity of misalignment direction for corresponding layers. V0-M1B and M1A-M1B OVL show similar edge elevation pattern, while V0-M1A is with uniform OVL profile (both V0A and V0B exposures). After optimization of lithographic process and overlay procedures, wafer maps of OVL errors are minimized and matched between both metal exposures V0-M1A and V0-M1B.

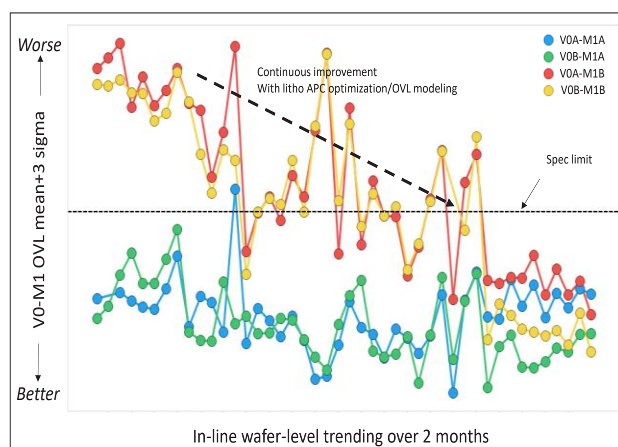

Fig. 3. Overlay trends for Dual-exposure Via to Dual-exposure Metal lines . V0A/B better OVL to M1A than to M1B. Time trend shows progress in OVL due to Continuous Process Improvement.

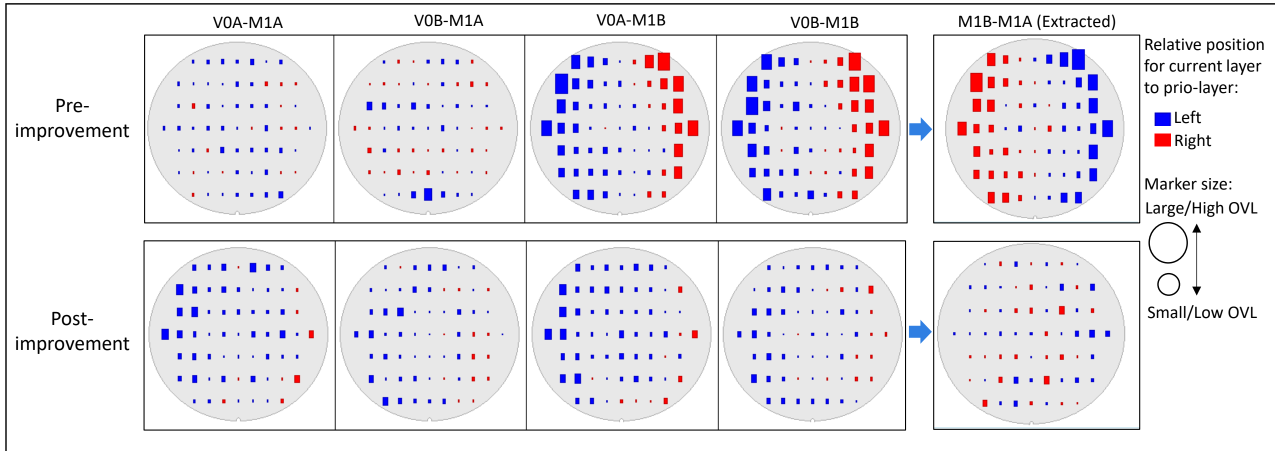

Fig. 4. Wafer Maps of misalignment values (OVL) measured with DFI structures. Larger marker size indicates larger OVL error, and the color shows the error sign (the polarity of misalignment direction for corresponding layers, see the legend). V0A and V0B - both Via exposures aligned directly to M1A pattern show good results with small OVL error, while the same V0 patterns show poor alignment to the second M1B exposure pattern. After improving lithographic process, OVL patterns are matched for V0 aligned to both M1A and M1B.

In addition to overlay metrology, DFI method can also measure Process Window and Process Margin (PM), as shown by the arrows in the plot of Fig.1. Process Margin is defined as a smaller of the two values from the center axis to the two arms of the OVL curve. In our case, the Process Margin is measured by the eBeam Voltage Contrast. PM variation is affected by both M1/V0 CD and their OVL. Analysis of the wafer-level spatial patterns, the regions with high risk of Via open and lower yield can be identified in fully built BEOL stack.

Fig. 5 shows PM wafer maps across 4 combination of V0-M1 colors, before and after litho process improvement discussed earlier. Narrow process margin for V0-M1B open is observed at edge of wafer due to poor V0-M1B OVL, and significant enhancement of the process margin is achieved after litho improvement. With DFI methodology, OVL and PM can all feedback to inline methodology to verify process-induced OVL bias post litho step and highlight any risk induced by CD and OVL variations.

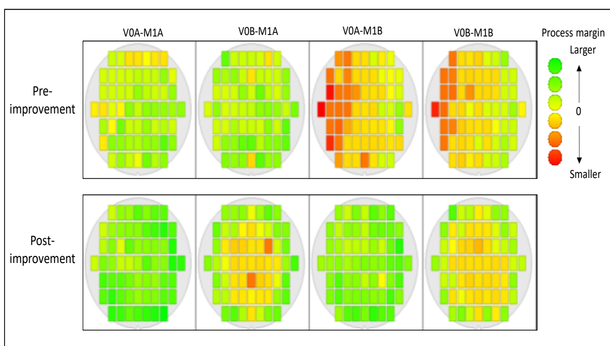

Fig. 5. Wafer maps of Process Margin for V0-M1 Opens by die, extracted using DFI structures. The window is very narrow when the alignment is poor, and improves with tighter OVL (RED very narrow Process Margin, GREEN is good)

Conclusions

This work demonstrated a new methodology of monitoring multi-patterning alignment scheme using eBeam-based DFI system. M1/V0 OVL and Process Margin examples proved applicability to detect OVL issues and support process improvement. In-line monitoring using DFI system was successfully applied to identify root causes of the narrow Process Margin and to drive process improvement. The proposed method can be extended to all BEOL layers and help control OVL and PM performance.

References

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