Expediting manufacturing safe launch with Big Data AI/ML analytic solutions on the cloud

Helen Yu [1], Scott Martin [1], Laurenz van der Meer [1], Edward Yang [2], Sherry Lee [2], Wanting Xiong [2]

[1)] Renesas Electronics Corporations, 6024 Silver Creek Valley Road, San Jose, CA 95138, USA

[2)]PDF Solutions, 2858 De La Cruz Blvd, Santa Clara, CA 95050, USA

Abstract

With highly competitive time-to-market and time-to-volume windows, IC suppliers need to be able to release new product to production (NPI) in a timely manner with competitive manufacturing metrics. Manufacturing yield, test time and quality are important metrics in NPI to Manufacturing safe launch. A powerful yield management system is crucial to achieve the goal metrics. In this paper, recommended yield management system selection criteria, data integration methodology and innovative ways of using selected yield management system to benefit safe launch efficiency are introduced. Three examples of using cloud yield tool to expedite yield learning, test time reduction (TTR) and quality enhancement are presented.

Keywords: *Yield Management System, Manufacturing, New Product Introduction (NPI)*

Introduction

Competition strength in semiconductor field depends on IC features, time to market, cost and quality.

Production yield, test time and Statistical Yield Limit / Soft Bin Limit (SYL / SBL) lot rejection rate (LRR) are important manufacturing metrics on cost and quality. Higher yield and lower test time allow IC suppliers to offer products at competitive prices while maintaining profitability. Consistent quality from optimized yield and quality excursion prevention enhances customer satisfaction, fosters brand loyalty and provides a competitive edge.

A fast and efficient safe launch to optimize yield, test time and quality from NPI to production can facilitate time to market and time to volume, which is crucial to the success.

Large IC suppliers (e.g. Renesas) typical have a big variety of products and large amount of manufacturing data, it is challenging even for skilled engineers to manually find informative patterns in the data to attain rapid yield enhancement and test time reduction for cost reduction and quality improvement.

A yield management system which can expedite the safe launch data analysis, by integrating large amount of data size and accommodating all types of users are needed for IC suppliers to achieve manufacturing excellence to remain competitive in the field.

In this paper, we introduced how to choose and use commercially available AI/ML cloud yield tools to achieve manufacturing excellence with fast safe launch results. Cloud yield tool evaluation criteria and roll out methodology are recommended. Three use examples are given on how to achieve fast safe launch results with better yield, test time and quality.

Safe Launch in Semiconductor IC Suppliers

When a new product is introduced and released to production, safe launch is desired to achieve better yield, test time and quality in a timely manner.

In safe launch, the first level of yield analysis is to monitor and compare the product yield with the target yield. If the yield cannot meet target yield, yield enhancement is required to achieve the standard cost yield. Fail pareto analysis on HB, SB and test numbers, wafer pattern and parametric distribution analysis are the first level of analysis.

Engineers will then isolate yield loss to all potential contributors, such as fab / foundry, test setup, test software, assembly and manufacturing sites. The second level of analysis involves in-depth analysis in the identified area. The fab / foundry data normally include inline data, WAT and equipment / recipe split and monitoring data. The test data include test hardware data (e.g tester, handler, load board, probe card, socket etc.) and test software (e.g test program revision, test hard and soft Bins, test numbers, parametric, wafer maps etc.). The data analysis requires a large amount of data from different manufacturing facilities with genealogy traceability.

This requires systematic data collection from varieties of manufacturing sites and / or subcontractors. To identify the low yield root causes, multiple correlation analyses from different manufacturing steps (e.g fab, assembly, test) are needed.

Test time reduction and yield enhancement can lower the IC cost. Retest reduction to achieve better OEE makes the manufacturing more efficiency.

SYL / SBL performance is a good indicator of quality, as it is found that SBLs can detect process shifts and reject misprocessed material [1]. A large amount of data to ensure statistical significance and, due to the possible non-Gaussian nature of bin distributions, statistical models are required for SYL/SBL calculations.

Genealogy information is required to aggregate and correlate different types of data measured at different stages of the manufacturing process.

Traditionally, engineers use excel or load the raw data to some statistical tools to complete the analysis, which is very time consuming. Even for experienced engineers, it isn't easy to complete the safe launch with meaningful results in a timely manner.

Yield Analysis Tools and Requirements

An IC supplier engineers typically utilize either home-grown yield tools and/or commercial tools for yield analysis and safe launch. Depending on the type of users of the tools, the

emphasis of the tools is different. For management and casual users, the overall yield reports and/or transactional analysis are used more frequently. Advanced users typically have more comprehensive requirements for the tool, including overall yield overview, transactional analysis and systematic yield improvement, drill-down and root-cause analysis.

Home-grown yield management system is customized for specific requirements from the company. This requires significant resource to continuous maintain and enhance the system for new requirements for new products, and slower to leverage learnings from the industry. Internal system often slow adoption of AI /ML methods and in-depth advanced analysis, the key focus for a semiconductor IT team is not to develop AI/ML yield management system.

As such is difficult for home grown tools to compete with the rapid development of commercial yield management system. There are pros and cons in different tools.

An ideal yield management system should be a system which can accommodate all level of users [Fig 1]. The system needs to be easy to learn and use (self-guided), can do automated analysis and reporting (e.g AI/ML) for engineering efficiency, at the same time have in-depth analysis capability; can customize to suit specific unique analysis needs, and is scalable when a company grows organically or with acquisitions, and is a cost-effective solution.

Exensio as a Manufacturing Analytics Platform

Exensio analytics platform is designed and architected to meet the needs of semiconductor supply-chain including wafer manufacturing, IDMs, foundries, OSATs and fabless companies. Exensio platform includes data acquisition, normalization, semantic and big data cloud management and semiconductor specific visualizations, analysis and reports. Also provide a platform to create and execute AI/ML models in real-time.

Exensio Guided Analytics (GA) is a module which uses advanced machine learning and artificial intelligence (AI) techniques to automatically diagnose root cause for wafer(s) categorized into different yield groups.

With the huge amount of data generated today in IC manufacturing, engineers usually only looked at 3-5% of the data and significant time spent aligning the data. Typically, only focus on obvious excursion and low yield, much less on systematic yield improvement. The goal for Guided Analytics is to continuously mine 100% of the data when various data types are integrated into the system while semantic date model automatically identifies data relationships. From analysis side, also automate 90% of analysis Product engineers, Test engineers and Yield engineers need. Even less experienced engineers can achieve the same analysis conclusions as seasoned engineers.

Customized analysis methodology can be plug-in to the system and allow ad-hoc drill-down analysis [Fig 3].

Examples of Successful Safe Launch

Three examples are given to illustrate how to use Exensio / Guided Analytic cloud tool for safe launch efficiency.

Exensio AI / ML Tool integration involves data integration with data format and manufacturing procedure standardization. This is essential for the data integrity and is the foundation of the yield tool.

Customized safe launch template with scoring system (Fig 4) was developed by using Exensio and implementing through GA for fast yield learning / improving, TTR and quality monitoring / improvement. This template was jointly developed by Renesas and PDF Solutions. The objective is to make engineers' safe launch data analysis more efficient. The implementation involves scoring products based on yield comparison with target yield, LRR (lot rejection rate based on SYL/SBL), test recovery and AI / ML assisted low yield analysis. Reports can be generated automatically and downloaded from the cloud server. This template generated the full report covering yield, quality and test time reduction in one stop.

Example 1[Fig 2]: Yield improvement with AI / ML in safe launch template. AI / ML algorithm automatically detects the low yield root cause. Seamless drill-down in the GA can verify the accuracy of the AI/ML. In the example, an edge pattern and correlation with a WAT parameter was detected with the AI / ML. Automatic meta data analysis helps to isolate the low yield issues to a specific area.

Example 2 [Fig 5]: Quality LRR monitor in safe launch template to monitor quality of the line. Lot rejection rate based on SYL/SBL is automatically calculated and compared with target goal. High LRR can be analyzed seamlessly with GA by using structured analysis. Special quality template can be built and save to GA as needed (e.g ECID template).

Example 3 [Fig 6]: TTR and retest recovery improvement in safe launch. Sorted failure pareto down to the test numbers. Easy to detect potential removal test items for TTR. Automatic retest recovery rate updates at SB level to help locate the area for improvement.

Conclusion

Completing a safe launch with competitive yield, test time and quality can take months or years' of engineers' time. It requires a large amount of data collection and big data analysis from different manufacturing facilities. Selecting a good yield management tool and use the tool efficiently will help the engineering efficiency to achieve manufacturing excellence in a timely manner. Deploying such system in a multi-cultural environment and a company with series acquisitions also provides an opportunity to standardize and improve operation efficiency.

References

[1] S. Illyes; D. Baglee, "Statistical bin limits: an approach to wafer dispositioning in IC fabrication", IEEE/SEMI Conference on Advanced Semiconductor Manufacturing, 1990.

[2] https://www.pdf.com/products/exensio-analytics-platform/overview/

[3] Hari Balachandran, Jason Parker, "Expediting Ramp-to-Volume Production", Proc. International Test Conference 1999.

[4] Kouta Nakata, "A Comprehensive 'Big-Data-Based' Monitoring System for Yield Enhancement, Symposium on Semiconductor Manufacturing, 2016.

Figure 1: Exensio Guided Analytic module can accommodate different levels of users

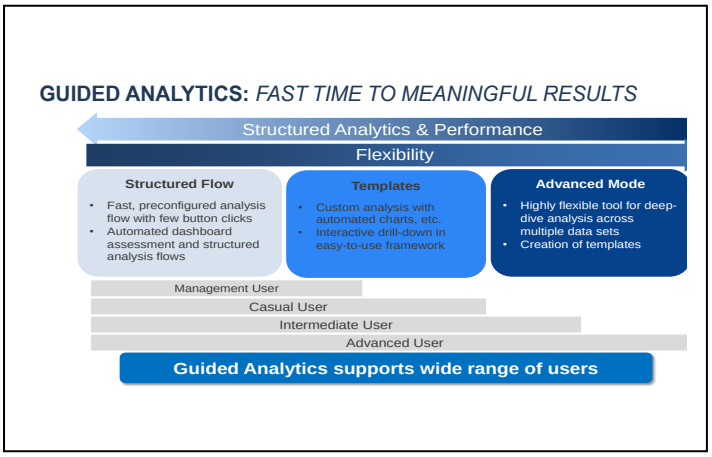


Figure 2: Exensio Guided Analytics module AL/ML automatically detected low yield wafer edge pattern with WAT parameter Vth root cause

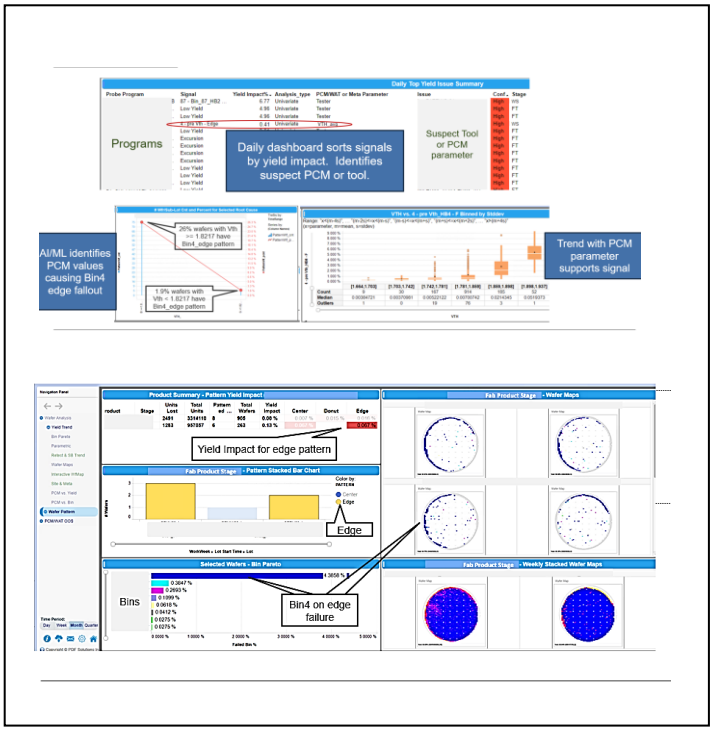


Figure 3: Seamless flow between Exensio and GA

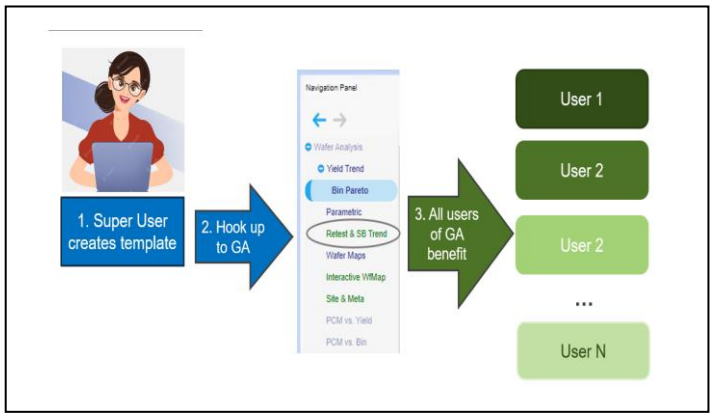
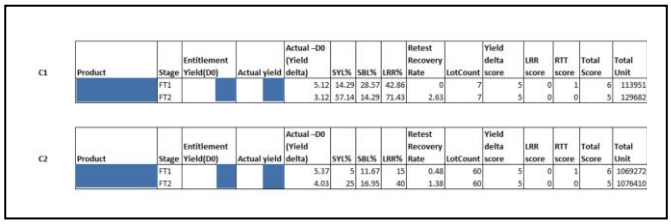


Figure 4: Safe Launch Template scoring based on Yield, LRR and Retest recovery



	Product	Stage	Entitlement Yield(D0)	Actual yield	Actual –D0 (Yield delta)	SYL%	SBL%	LRR%	Retest Recovery Rate	LotCount	Yield delta score	LRR score	RTT score	Total Score	Total Unit
C1		FT1			5.12	14.29	28.57	42.86	0	7	5	0	1	6	113951
		FT2			3.12	57.14	14.29	71.43	2.63	7	5	0	0	5	129682
C2		FT1			5.37	5	11.67	15	0.48	60	5	0	1	6	1069272
		FT2			4.03	25	16.95	40	1.38	60	5	0	0	5	1076410

Figure 5: Safe Launch Template with automatic LRR monitoring (Lots violating SYL/SBL highlighted with

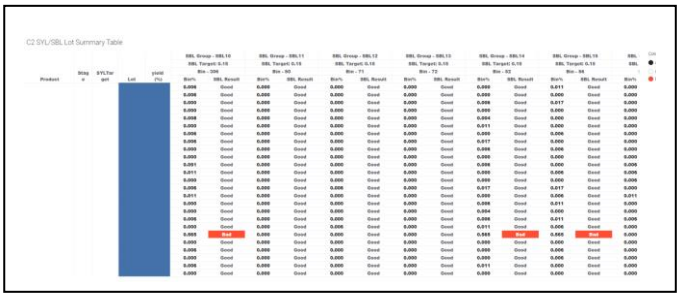


Figure 6: Safe Launch Template with TTR and Retest recovery opportunity findings