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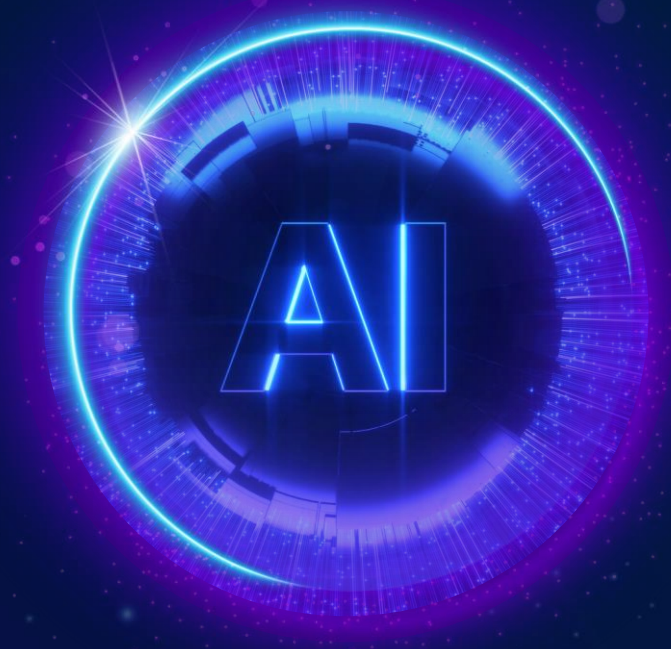
Artificial Intelligence

Executive Conference

explore the power of AI to transform semiconductor design & manufacturing



AI-Enabled Digital Twins for Equipment

Patrick Pannese, PDF Solutions
Aalhad Deshmukh, PDF Solutions
Anton Devilliers, TEL

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Over 200 Cimetrix Customers Including...

55K+ Equipment Installs & 150K Factory Connections!

Cutting-Edge Solutions for Semiconductor Innovation

CIMControlFramework

- Equipment control software toolkit
- Streamlines equipment integration and automation

DΣΣP

- Diagnostically Enhanced Equipment Protection
- Enhances equipment reliability and reduces downtime

Digital Twin “EquipmentTwin”

- Real-time digital replica for predictive maintenance and optimization
- Improves operational efficiency through data-driven insights

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CIMControlFramework (CCF)

The Ultimate Equipment Control Toolkit

- **High-Quality Development:** Enables high-quality equipment control application development
- **SEMI Standards:** Implements all SEMI equipment automation software standards
- **Out-of-the-Box Functionality:** Provides out-of-the-box functionality for typical equipment applications
- **Data Gathering:** Enables data gathering to support AI/ML integration
- **Health Indicators:** Includes health indicators to monitor component performance and report excursions.

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01.

DEEP - Diagnostically Enhanced Equipment Protection

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DΣΣP, Diagnostically Σnhanced Σquipment Protection

AI/ML Powered by PDF Solutions
- Industrial Hardened AI/ML
  - Currently in use in Tier-1 Factories
  - Many years experience with AI/ML
  - Equipment Focused AI/ML

Provides a Higher Level of Equipment Reliability and Deeper Visibility into Equipment Performance
- Ability to Check Overall Equipment Health
  - Overall Equipment Health & Characterization
  - Monitor Critical Equipment Sub-Component's Health
  - Create Golden Fingerprints for Each Sub-Component
- Predict Failures Before They Happen
  - AI/ML Monitors and Identifies When Component Health Starts to Deteriorate Over Time
  - Prevents Costly Unscheduled Tool Downtime

Enables a new flow of recurring revenue from services contracts

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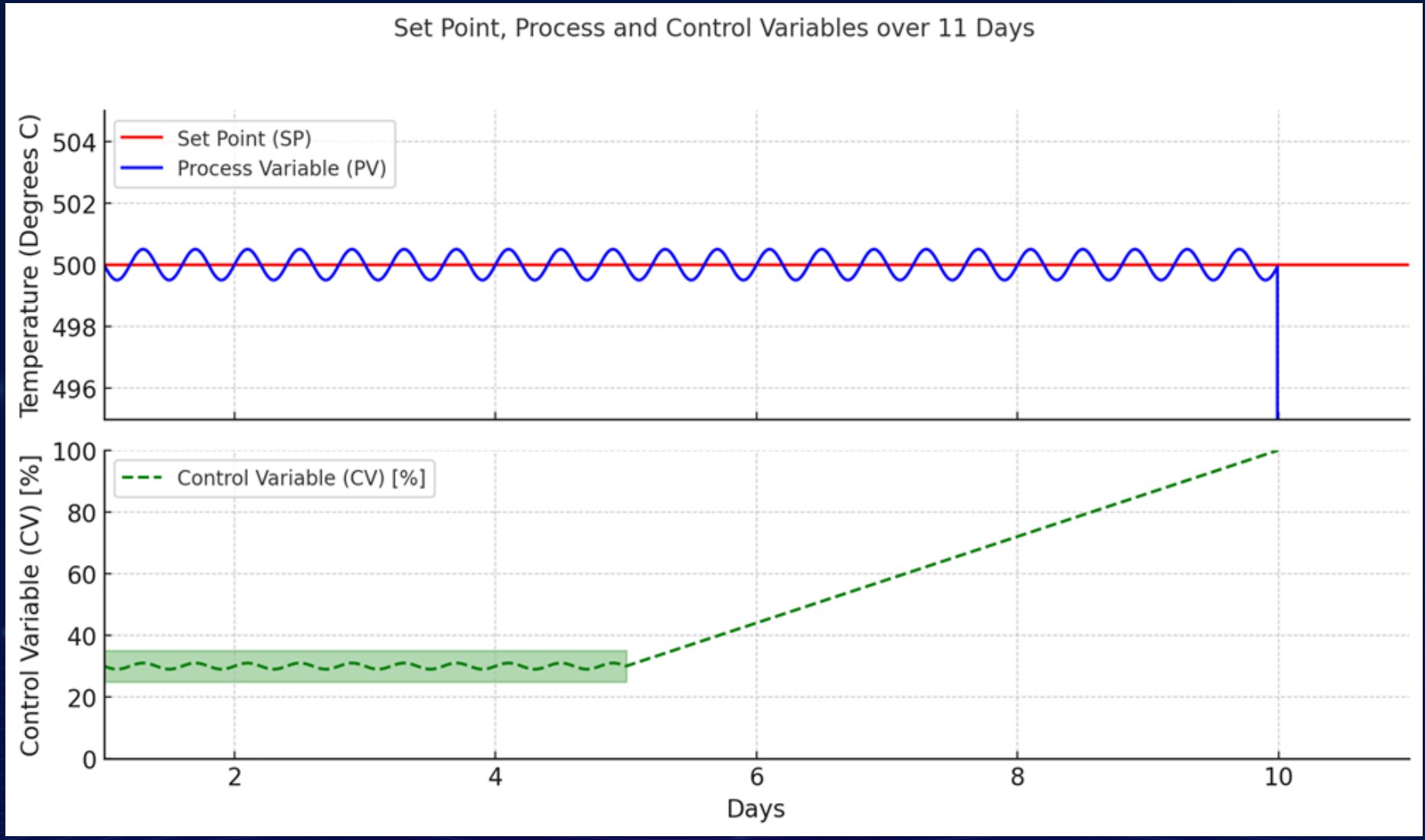
Simplified DΣΣP Heater Example



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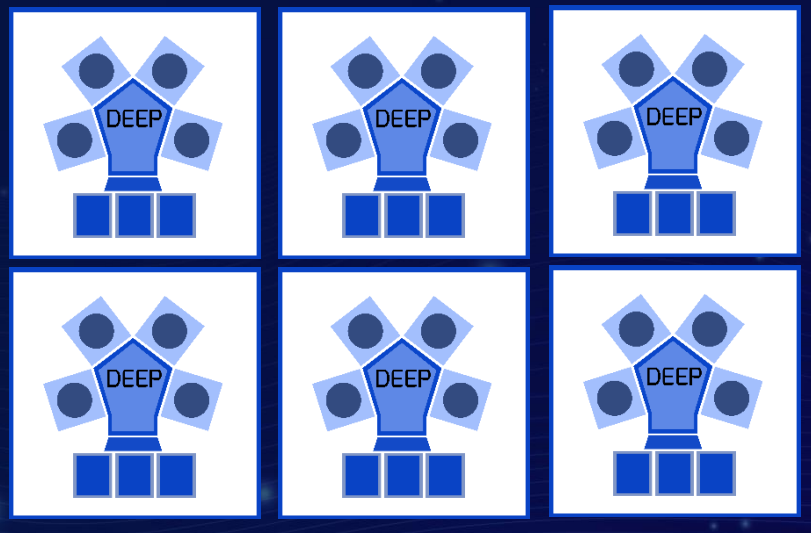
Value Capture During Life Cycle Testing

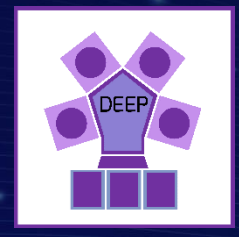
Equipment Manufacture Factory

- Equipment qualification and fingerprinting dashboardsyy
- High volume data access
- Independent edge box not impact tool operating system and performance
- Equipment fingerprinting
- Equipment matching and qualification
- Historical storage of all equipment fingerprinting to be used/sold at anytime



Foundry OSAT

- Equipment diagnostic and health dashboards for foundry/osat engineer
- Encrypted data
- Secured Linux operating system
- Diagnostic data for equipment support team by comparing golden fingerprint and current fingerprint of equipment
- Alarms and events published to foundry/osat engineer when equipment health issues are detected
- Fingerprinting of equipment to extend equipment PM cycles
- Equipment matching
- Move-in equipment qualification
- High volume data access API for building applications on the edge
- Protection for equipment proprietary data
- Equipment and foundry proprietary data is encrypted and only accessible with proper credentials
- Independent edge box not impact tool operating system and performance



DΣΣP, Robot ROI Use Case

- Robot Use Case
  - MCBF – 11,000,000
    - Assuming 24/7 1 cycle/sec implies 86,400 cycles per day
    - Failure every 127 days if no PM thus schedule PM every 90 days
    - 1 Day for PM on a 300wph equipment would cost 7,200 wafers at $3,000 per wafer implies $21.6M per PM or 4 PMs per year or total cost of $86.4M
  - Predict Failures Before They Happen
    - Golden Robot Fingerprints Would allow less frequent PMs
    - If Increase to 120 days or 3 PMs per year Fab saves 1PM or $21.6M

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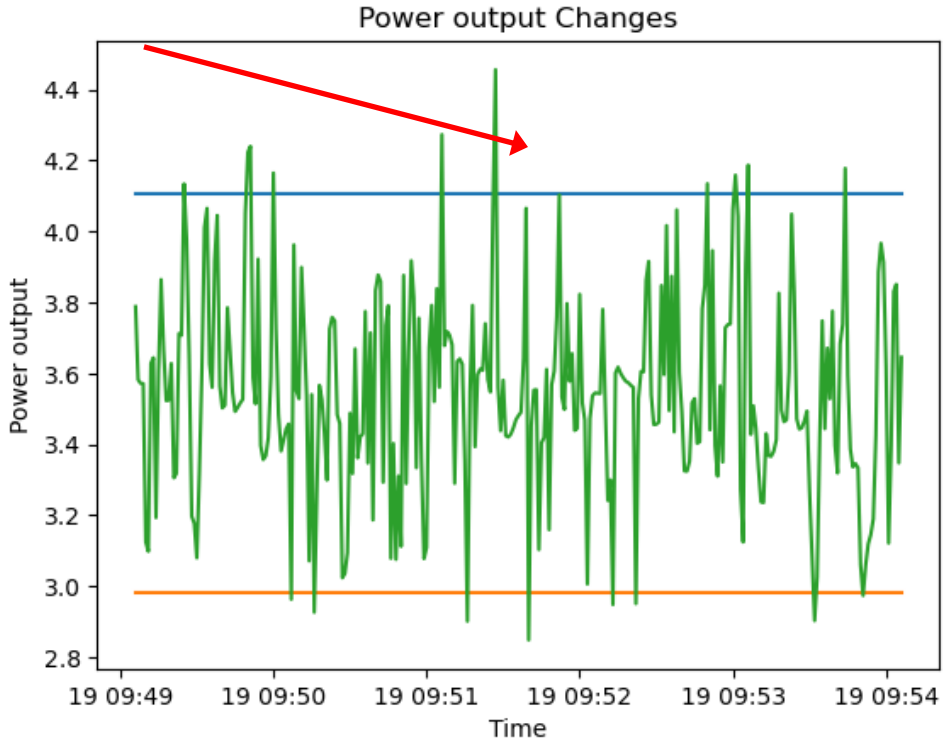
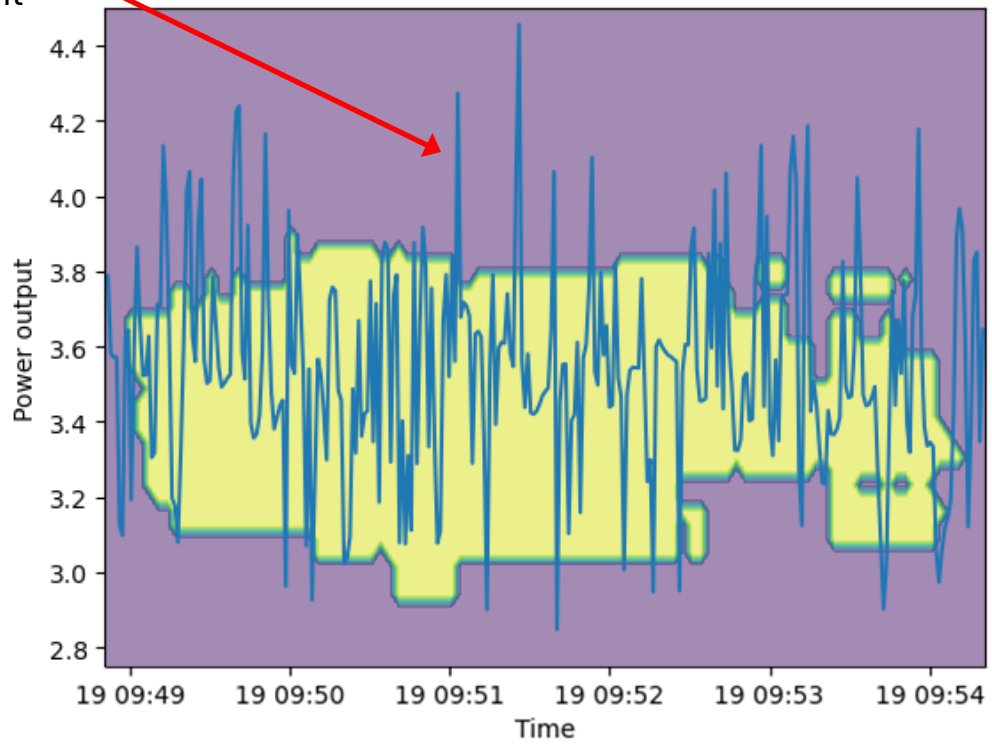
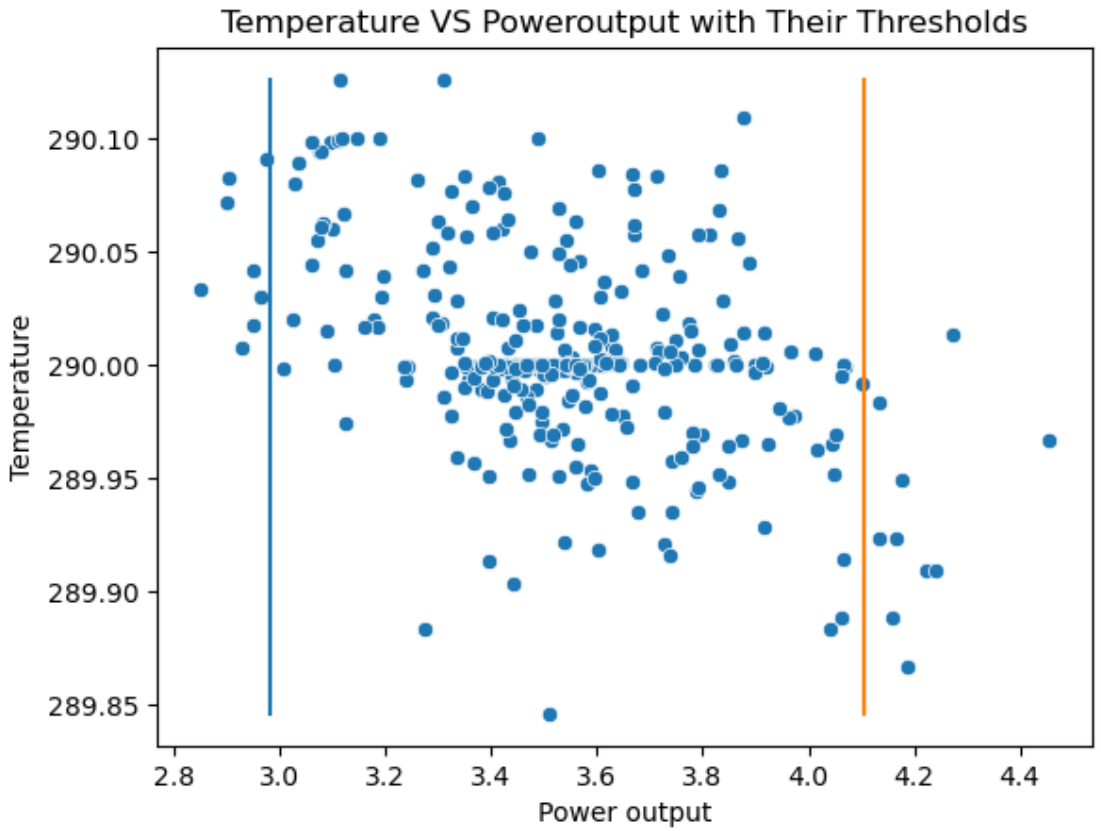
Abnormal Behavior Detection for Control Variable



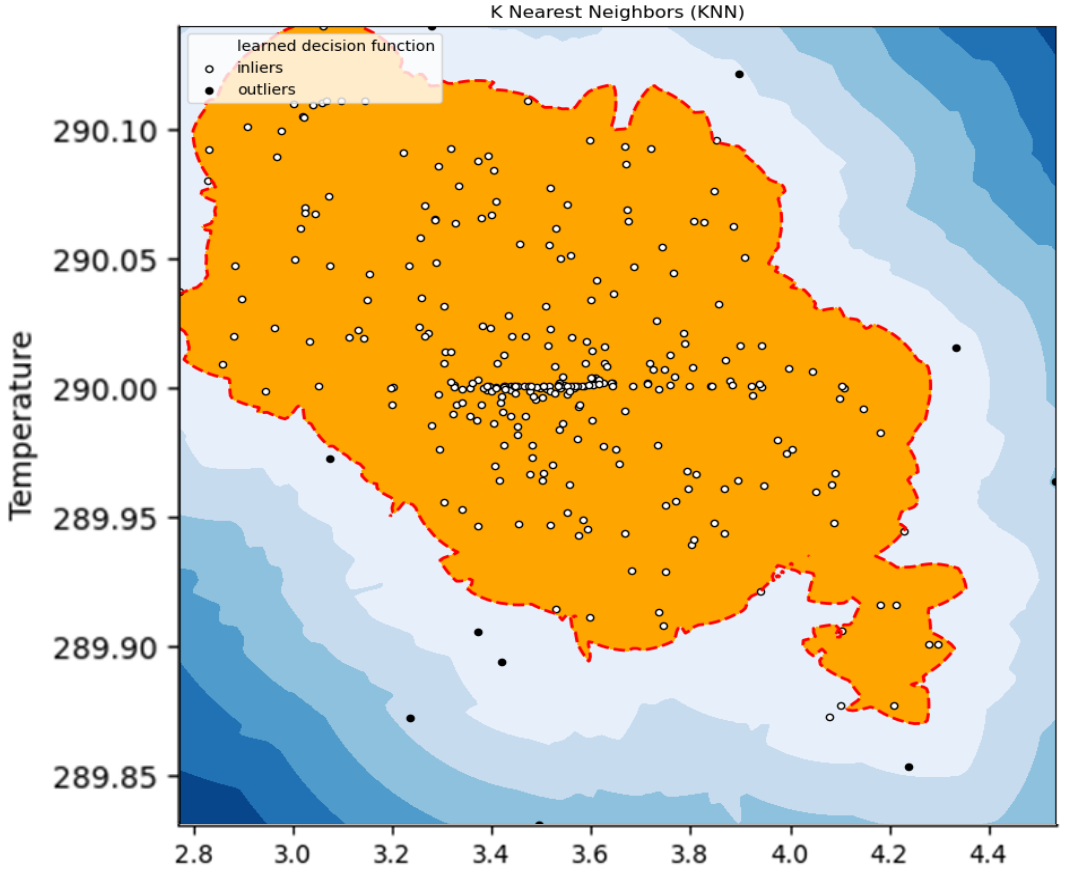
Abnormal behavior detection based unique fingerprint



Abnormal Behavior Detection for Combined CV/PV

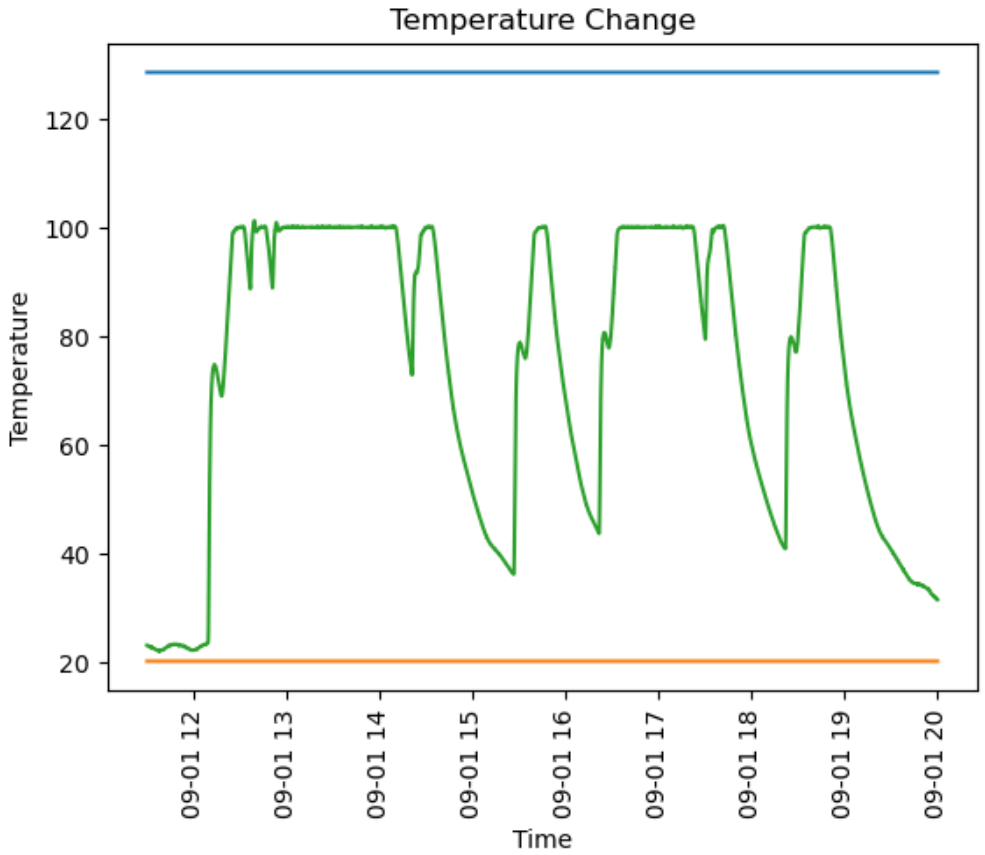


Traditional SPC approach doesn't reflect the correlation between CV (control variable) and PV(process variable).

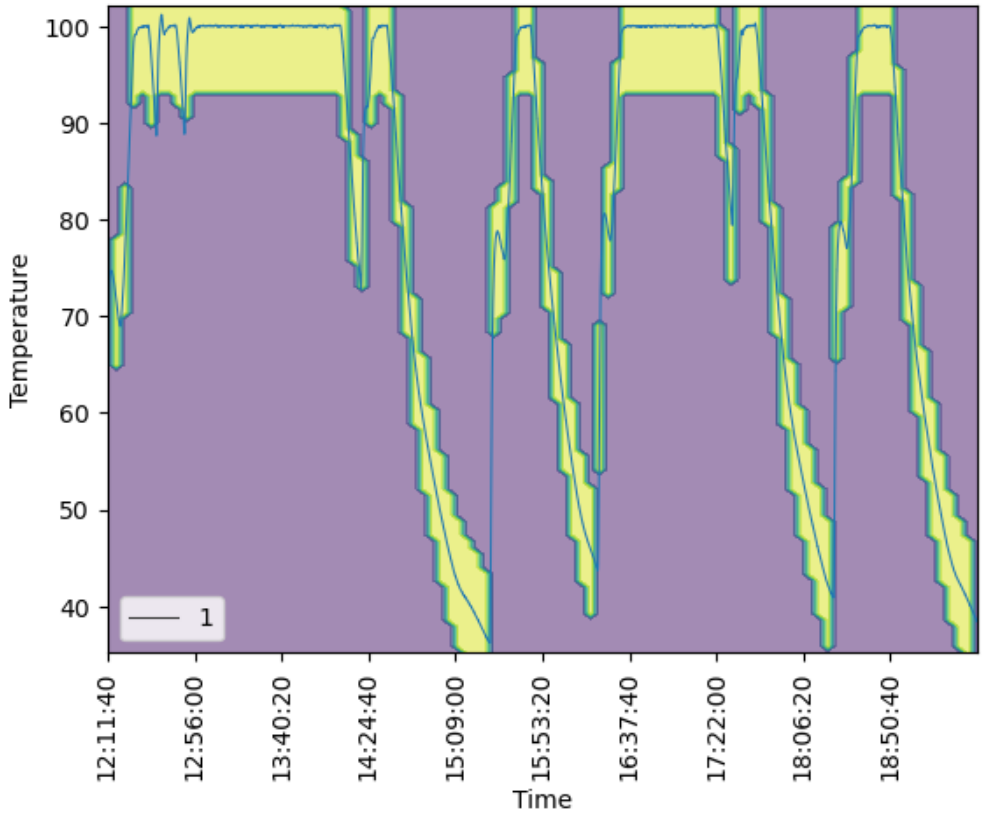


ML model can reflect the correlation between CV and PV, and creates a unique fingerprint of the unit, and detect abnormal behavior based on the fingerprint.

Statistical Approach vs. ML Approach

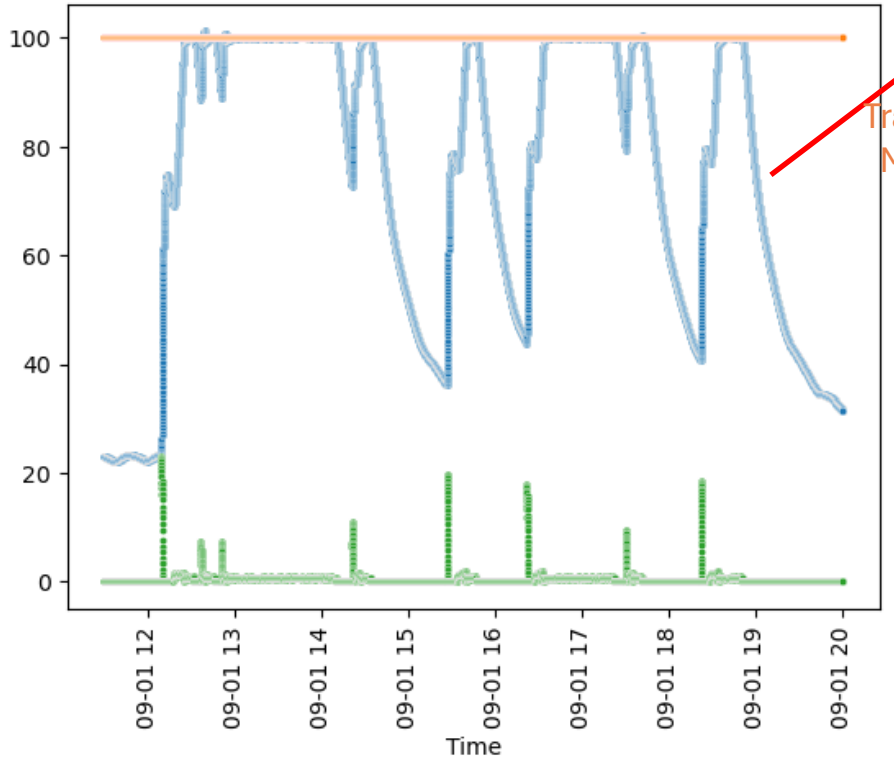


Traditional SPC approach can’t provide meaningful information when the values changes in multiple operation stages.



ML model learns the changes of the values and provide boundaries based on multiple operation stages. ML can help us find complex relationships between the input features that would've been hard for an expert to do manually.

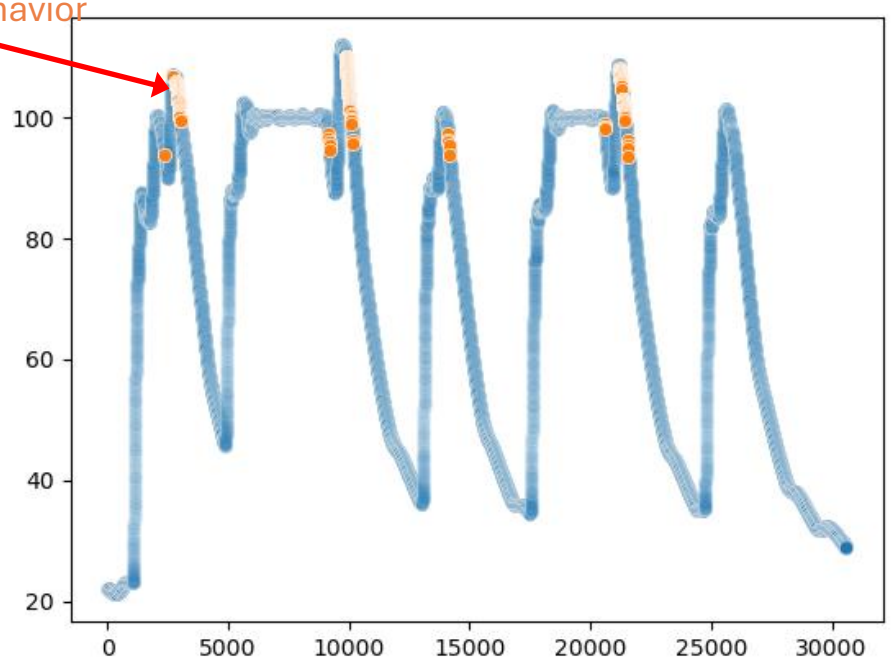
Outlier Detection using Novelty Algorithm



Train ML Model

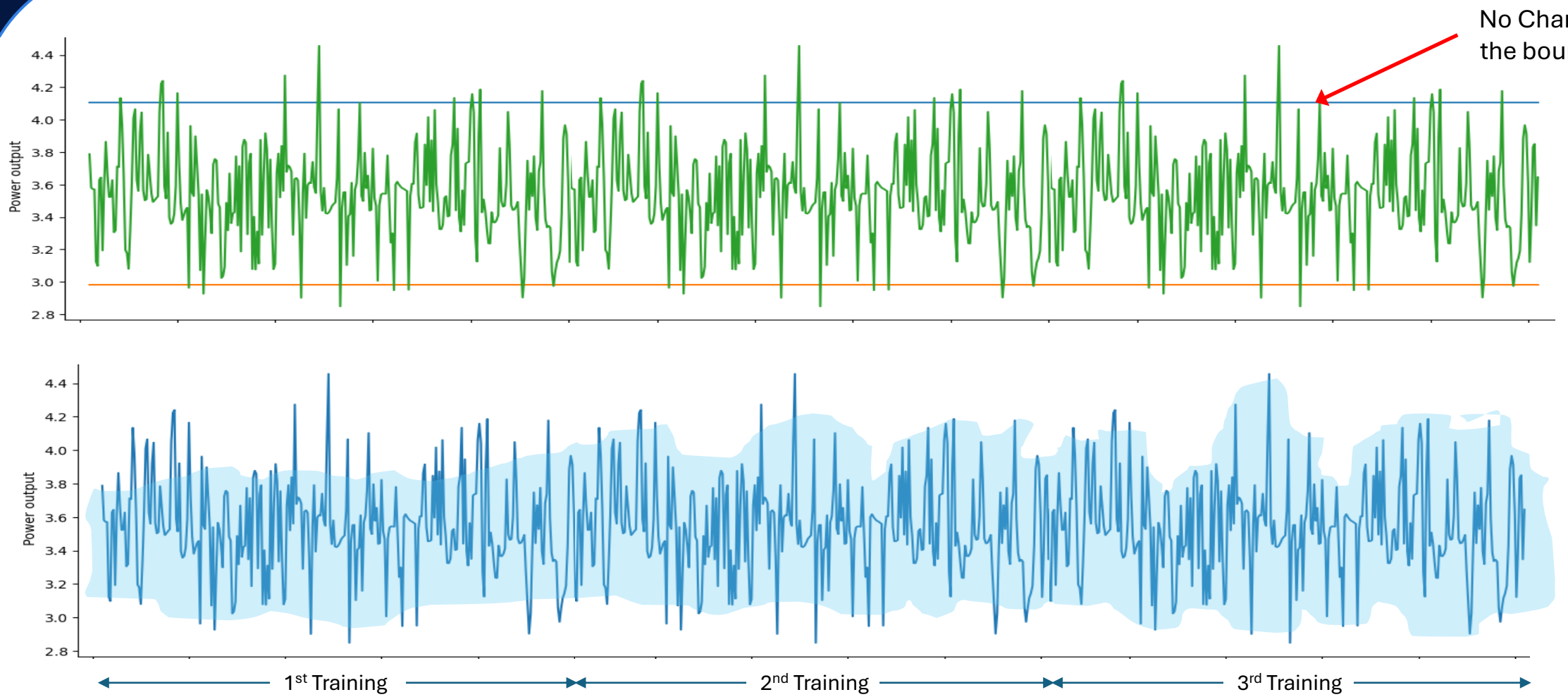
ML Model of Unique Fingerprint

Detect abnormal behavior



ML model compares new data against trained model and detects abnormal behavior when (different from the fingerprint) behavior.

Advanced Fingerprinting



ML learns unique behavior and adjust boundary for outlier detection

02.

Anomaly Detection using eProbe dataset

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Design-for-Inspection ™ (DFI) system at PDF Solutions

Detect the Undetectable

- What is DFI?
- How does it work?
- Early Visibility into Potential Risks
- Production-Proven

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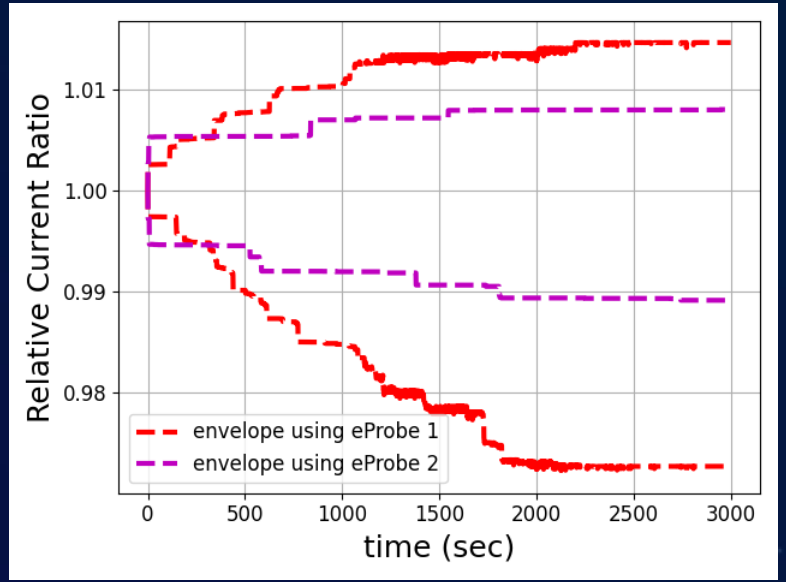
Anomaly Detection for eProbe using Envelope approach

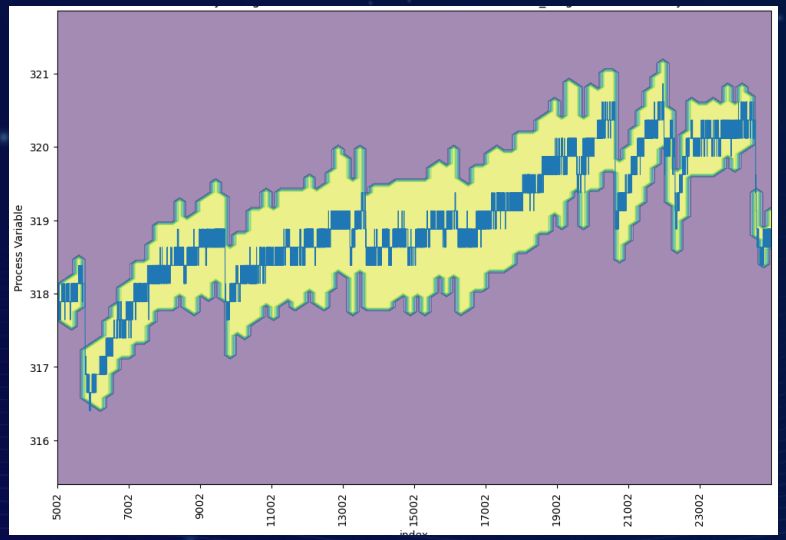
Envelope from two different tools at Fab

There are few existing anomaly detection algorithm for time series dataset. We will utilize Envelope approach to define the boundaries for normal traces during steady state. This is chosen given that we know ideal trace a priori as a horizontal line at y=0.

- The top right chart shows the envelops for two equipment based on the ratio of Heating Current and Emission Current.
- The bottom right chart shows the envelope from the dataset of Emission Current. (the ratio is used underneath)

Both charts show envelopes (boundaries) of the data from the different views. The result of anomaly detection will not be much different for a given specific data.





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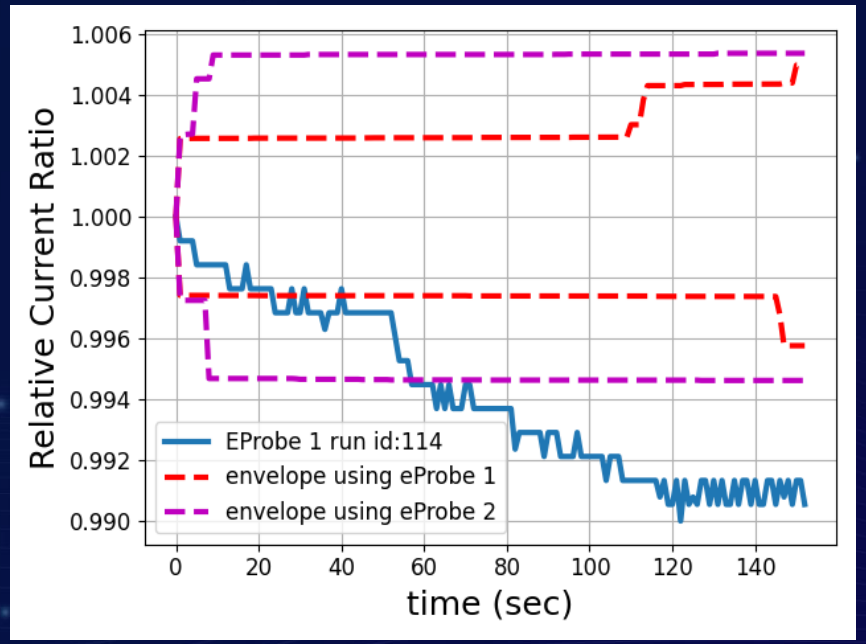
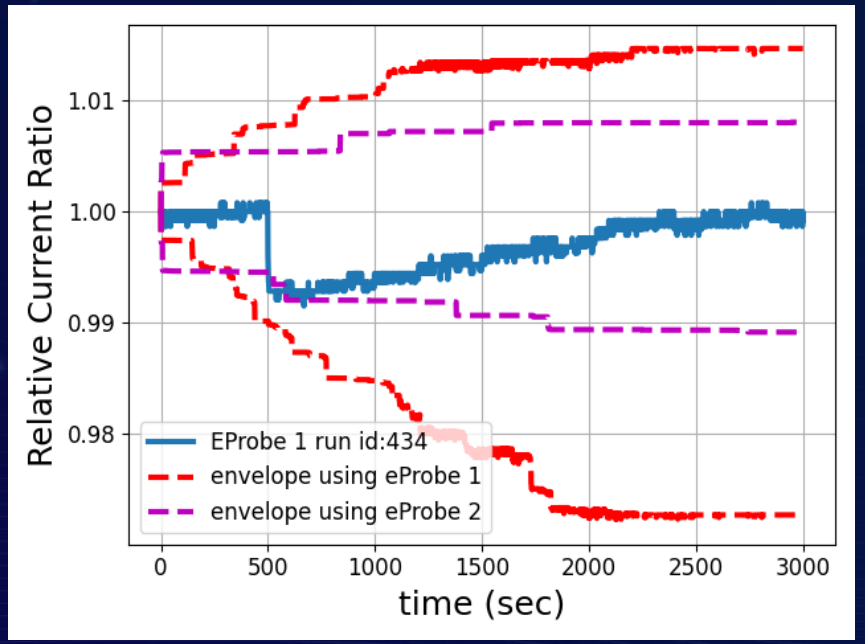
Anomaly Detection for eProbe using Envelope approach

Result

By using the Envelopes, abnormal situation can be detected. In the anomaly example, below the trace shows process has been terminated early. With envelop approach, we could have detected anomaly earlier.



Anomaly



Normal

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03.

Equipment Twin

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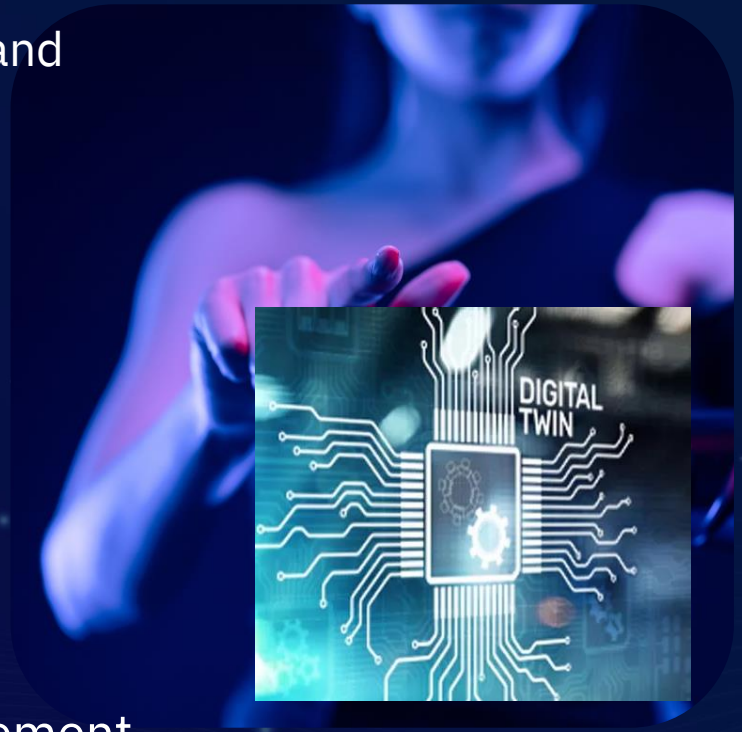
Harnessing Digital Twins for Operational Excellence

01 **Virtual Model:** Real-time simulation for predictive maintenance and optimization.

02 **Efficiency:** Explore, analyze, and optimize designs

03 **Time to Market:** Accelerate Development

04 **Continuous Improvement:** Ongoing monitoring and enhancement



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04.

Equipment Twin - Demo

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05.

Where do AI and Semi Eclipse - TEL

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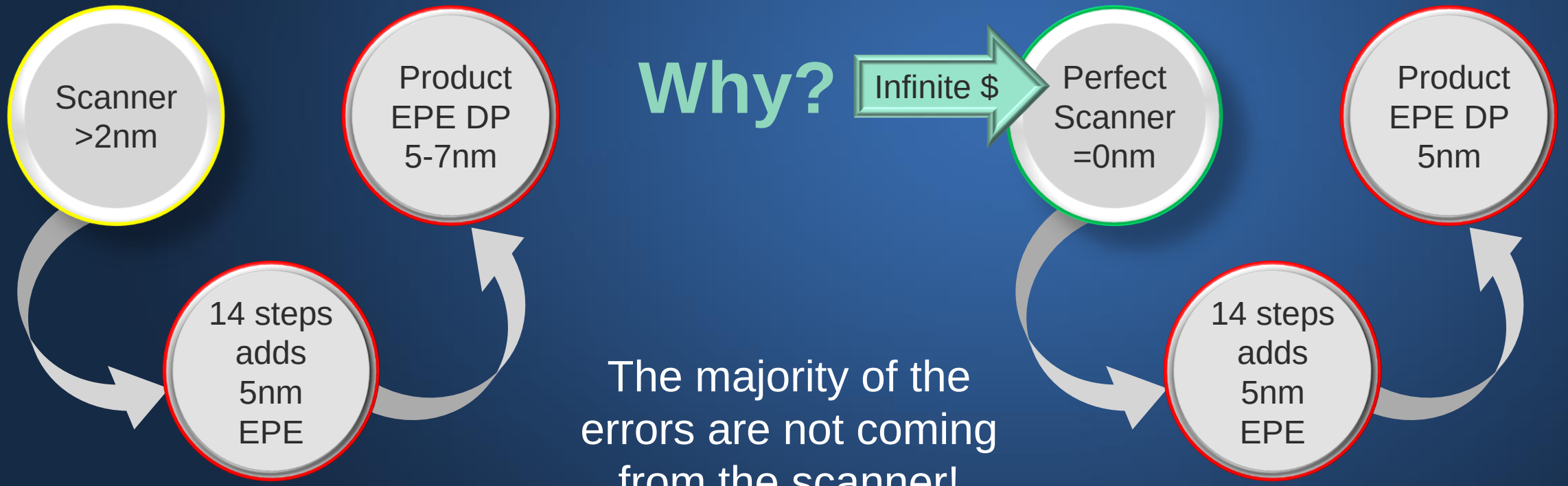
Where do AI and Semi Eclipse
TEL™

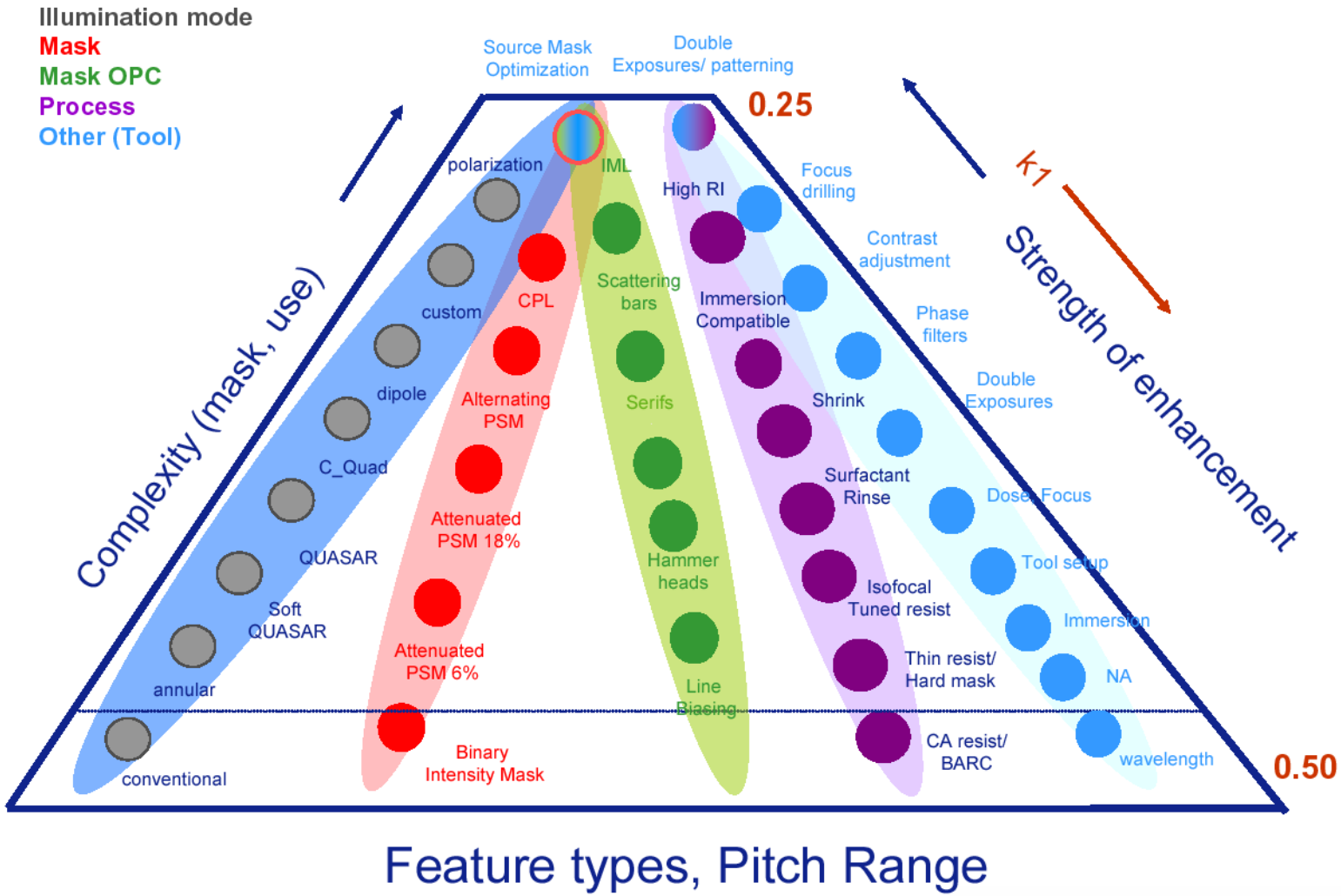
Why is it important to work in the digital twin space between tool makers

- Scanner makers can spend an *infinite* amount of money and make a *perfect* EUV scanner and the industry will not make the required 3nm EPE specifications on the product.

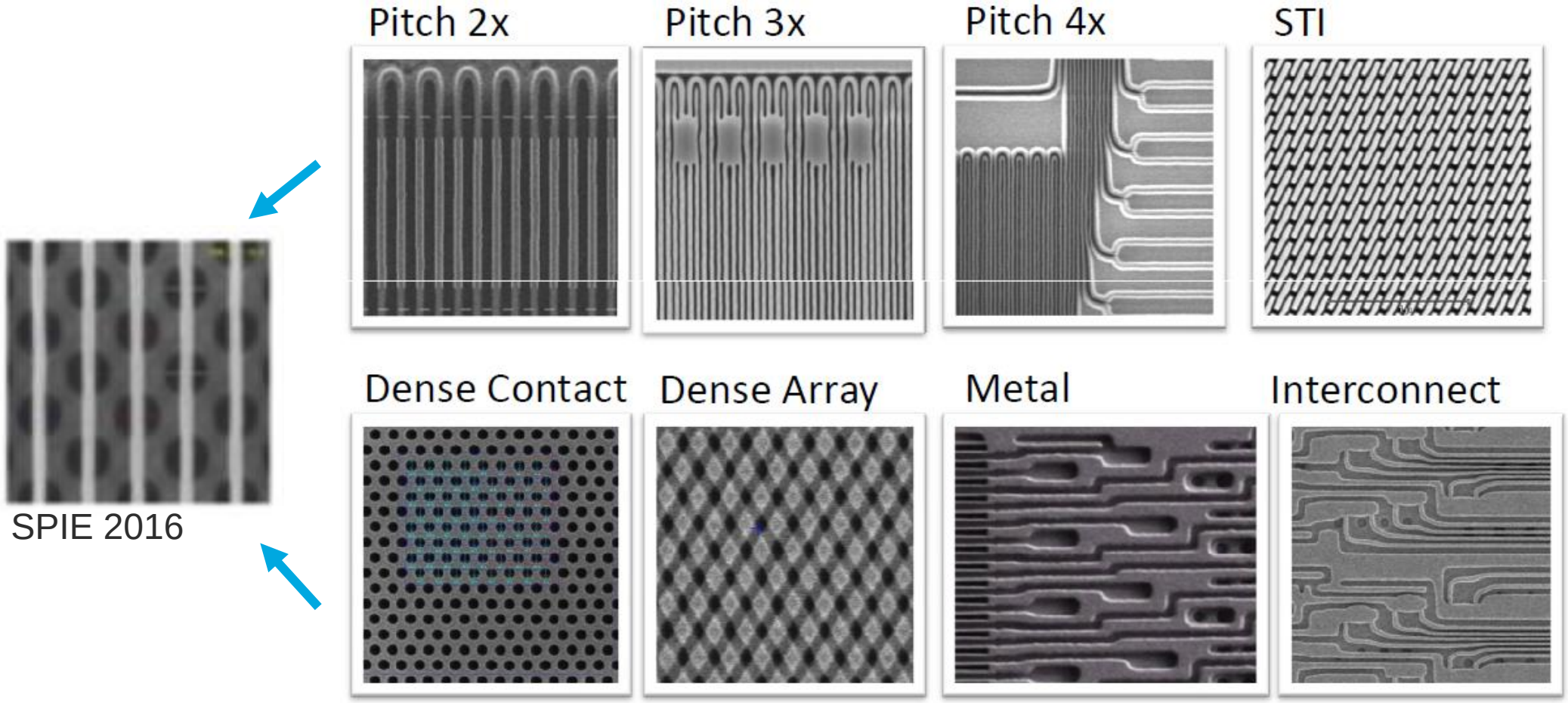


The majority of the errors are not coming from the scanner!

When Litho was simple and the dinosaurs left footprints in the earth, K1 ruled under King Raleigh

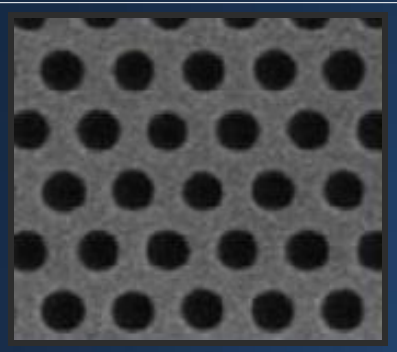


Bad old days of 2D vintage 2009-2012 RnD

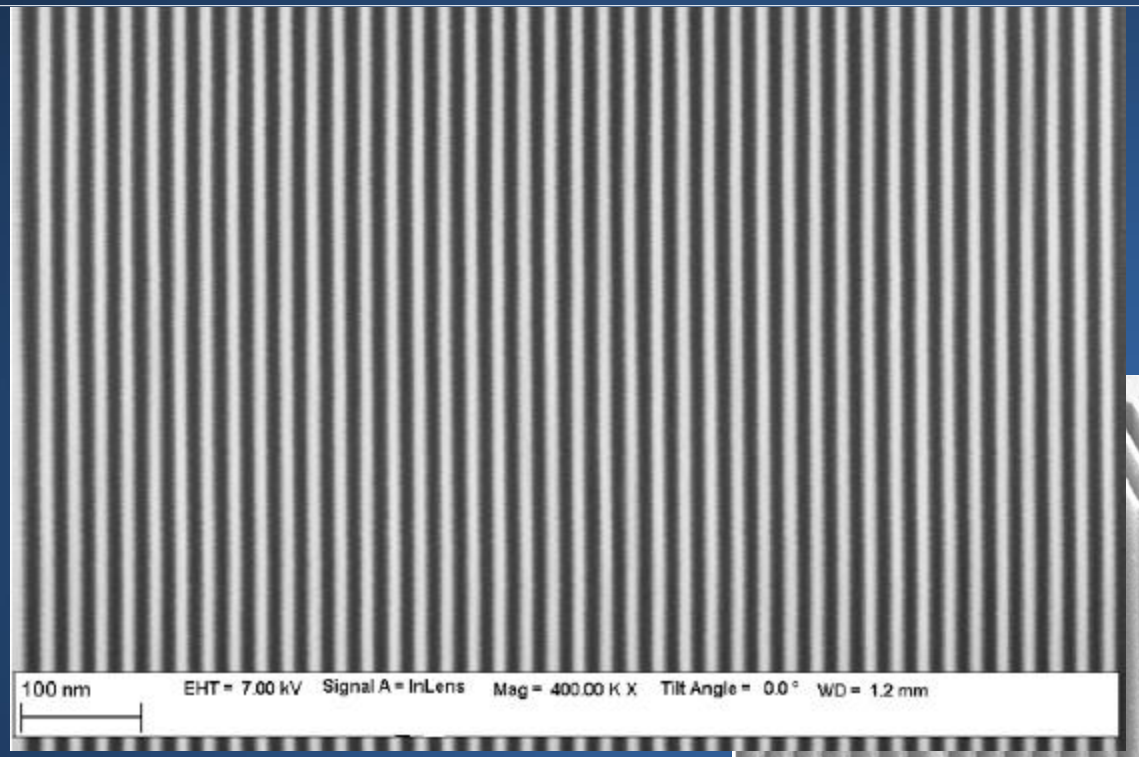


Published by Micron SPIE 2015

Benchmarks (Q4 2012- Q1 2013) is Awesome SI Enough?

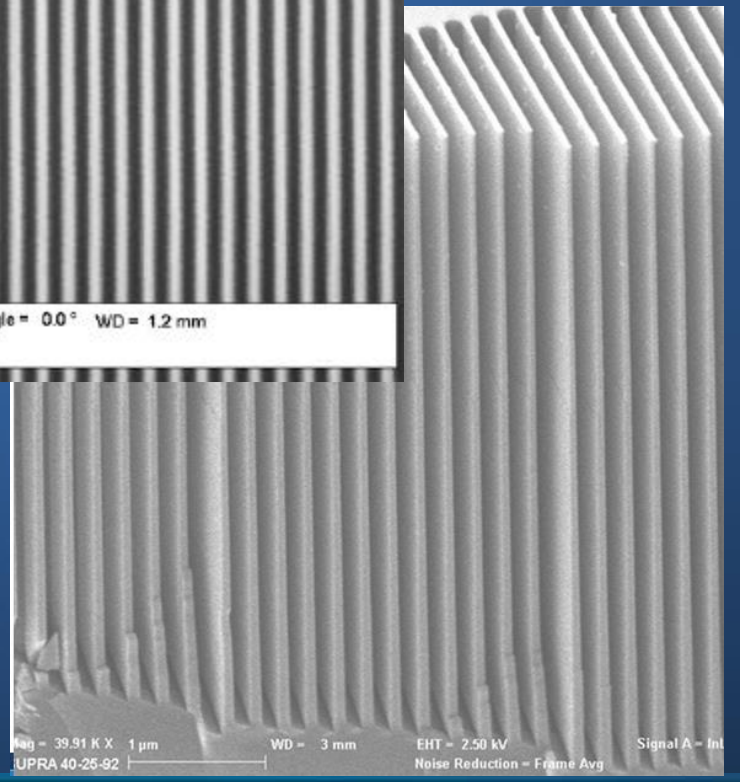


2Xnm CT's 0.9 LCDU



10nm L/s Wet Dev

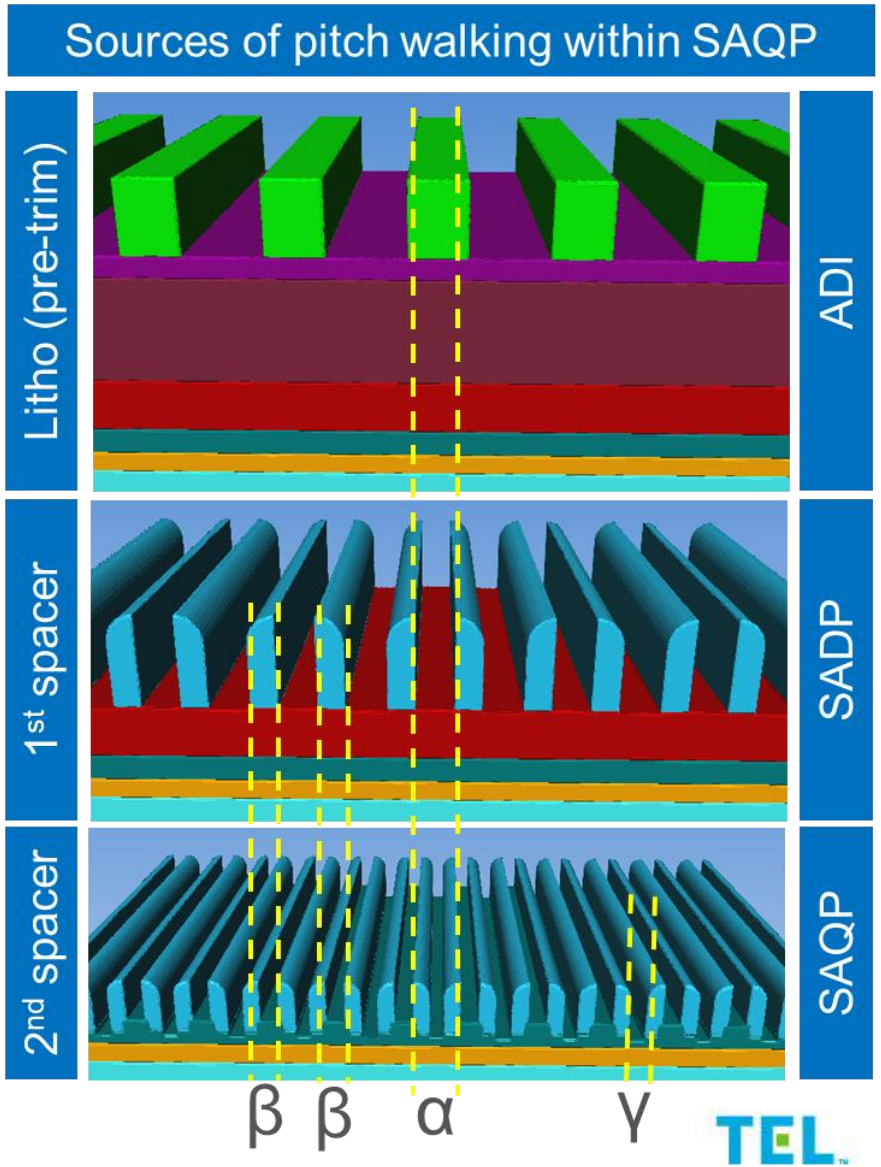
What future toolset will be needed
To support advanced Patterning
Applications?



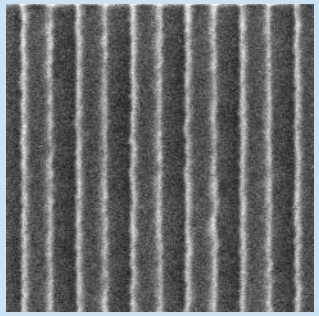
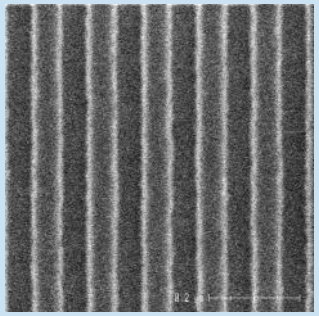
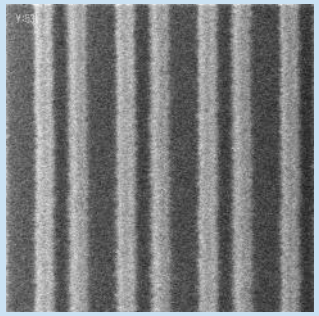
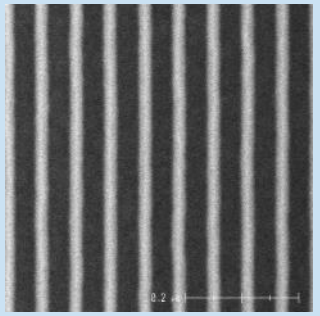
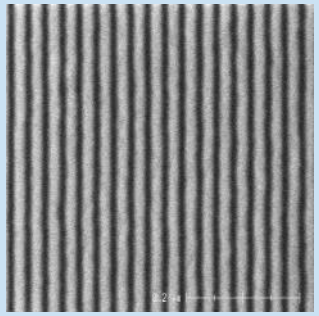
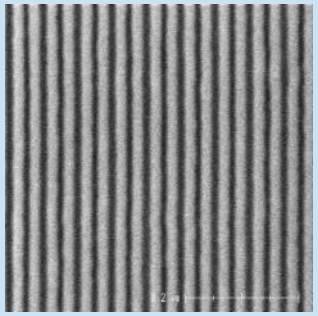
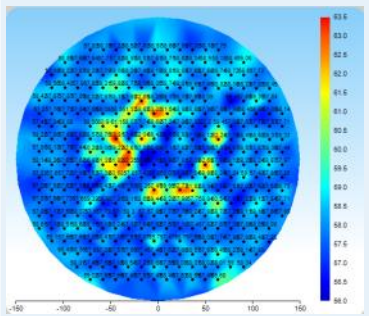
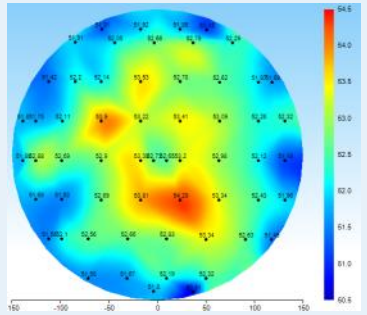
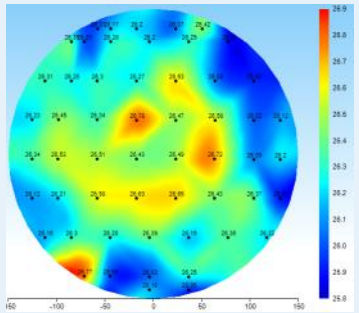
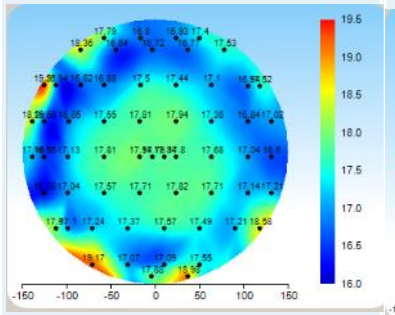
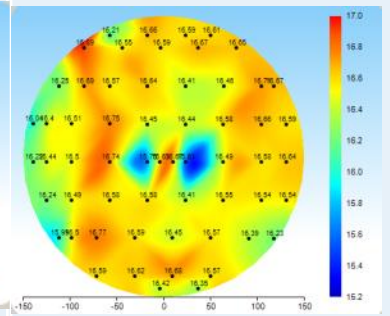
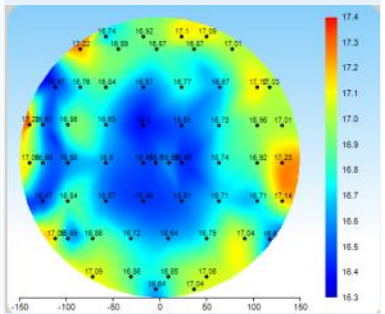
200:1
Aspect Ratio
Etch

What is Pitch Quad / Pitch walking

- CD variation of core(α) cause space size variation
- Average across wafer can be easily tuned by APC
- Uniformity of pitch walking
  - All source of CD non-uniformity
    1. Lithography (ADI) + top mandrel etch (AEI) ‘α’
    2. Top SPR dep/etch + Bottom MND etch ‘β’
    3. Bottom SPR dep/etch + TiN HMO etch ‘γ’
- 9% CD variation in the original ADI/AEI pattern can induce a 27% CD variation in final SAQP pattern
- Majority of problem can be solved by core uniformity



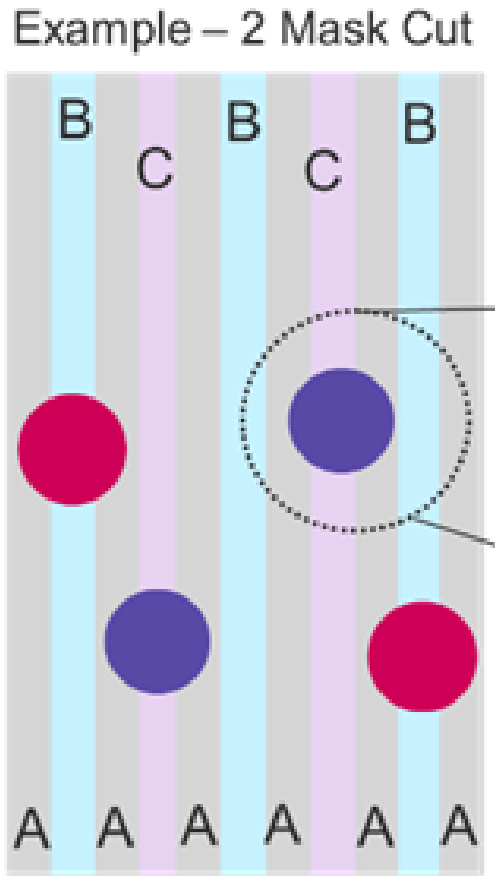
SAQP Process CD Partition

Litho	PR Trim (H2)	SEMP-1	Si Mandrel	Ox HMO	SiN HMO
					
					
CD: 58.7 CDU: 3.87 LER: 4.7 LWR: 4.7	CD: 52.3 CDU: 2.2 LER: 2.6 LWR: 3.3	CD: 26.2 CDU: 0.67 LER: 2.2 LWR: 2.3	CD: 17.5 CDU: 1.8 LER: 1.6 LWR: 1.6	CD: 16.5 CDU: 0.69 LER: 1.2 LWR: 1.8	CD: 16.8 CDU: 0.68 LER: 1.2 LWR: 1.7

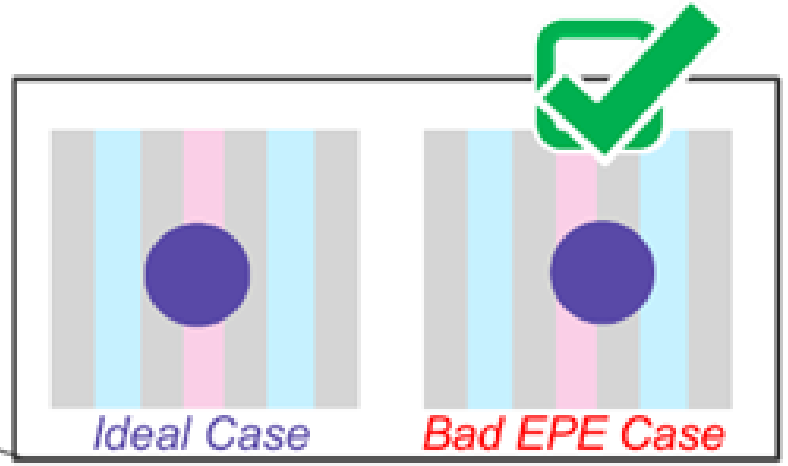
How does self aligned block work?

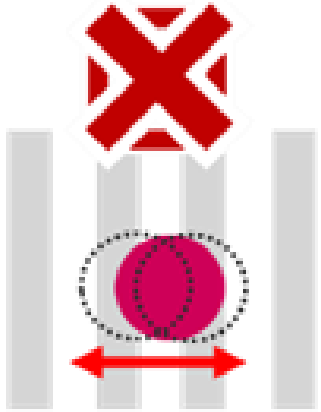
Etch system + Etch selectivity = Overlay

Self Aligned Block (SAB) concept



Every other trench has **different** fill material (**material with different etch selectivity**)





$$\sigma_{EPE} = \sqrt{\sum_{i=1}^{n}\left(\frac{\sigma_{CD-i}}{2}\right)^2 + \sum_{j=1}^{n-1}\sigma_{Overlay-j}{}^2} - \eta(x,y)$$

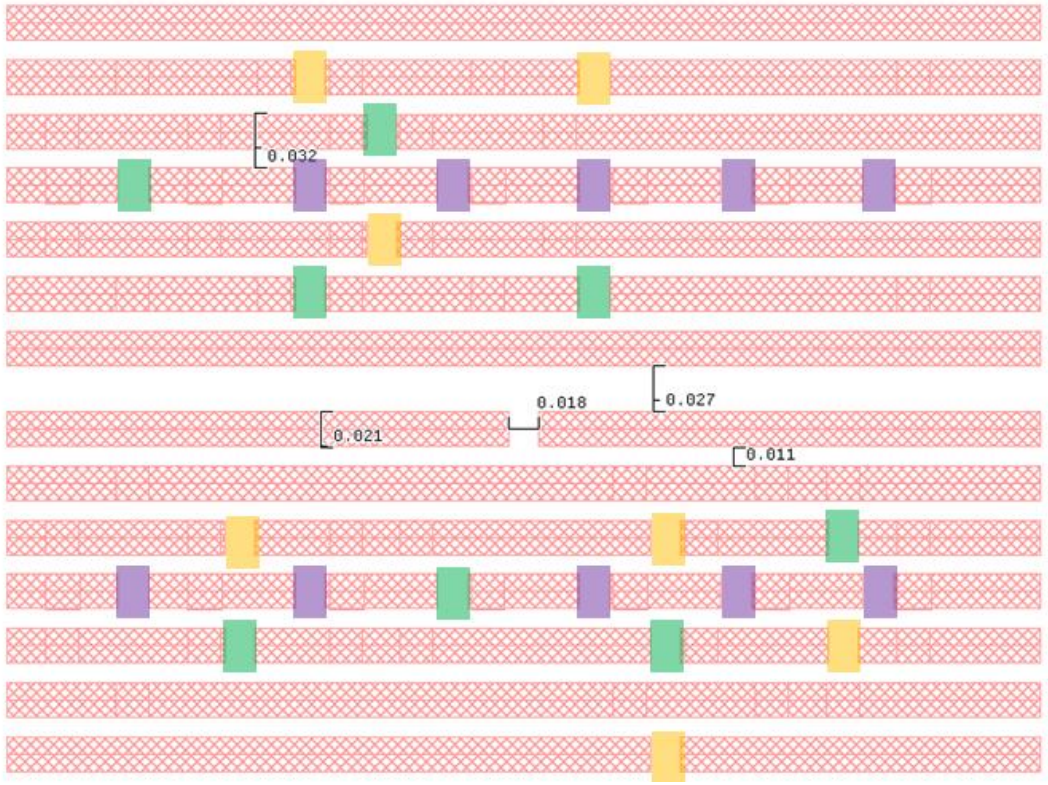
Overlay Improvement term

3X Relaxation in Overlay enabled thru self-alignment

Angelique Raley Self-Aligned Blocking Integration Demonstration for Critical sub 30nm pitch Mx Level Patterning with EUV self-aligned double patterning SPIE 2018

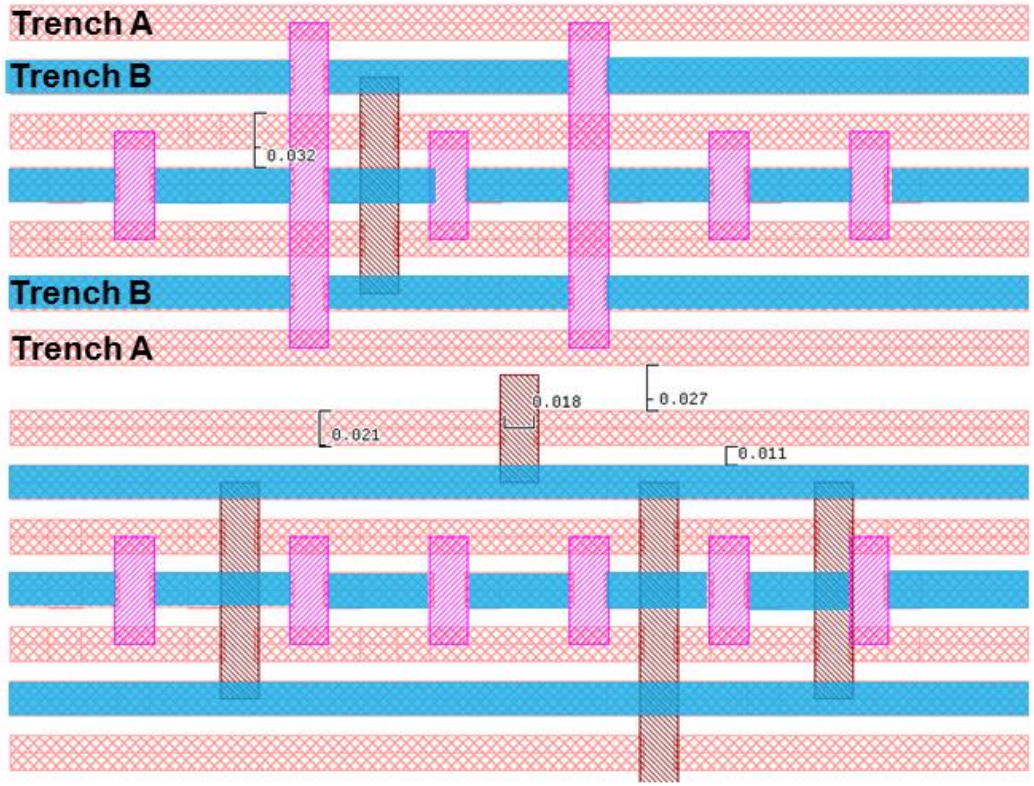
Self-aligned block for EPE control and mask count reduction

Conventional LE^3 block



EPE tolerance in y-orientation = ¼ pitch

Self-aligned block w/ multi-color etch

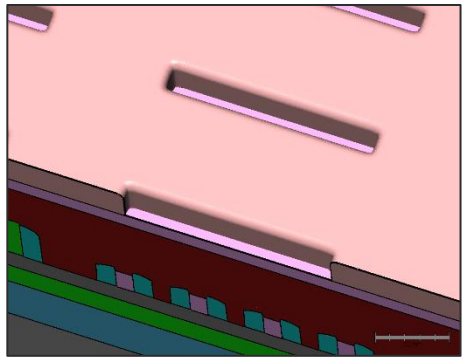
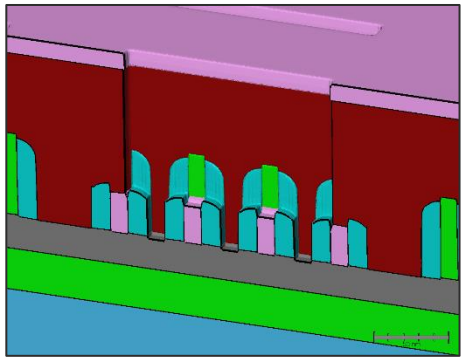
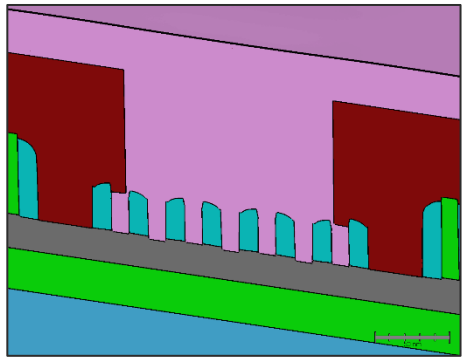
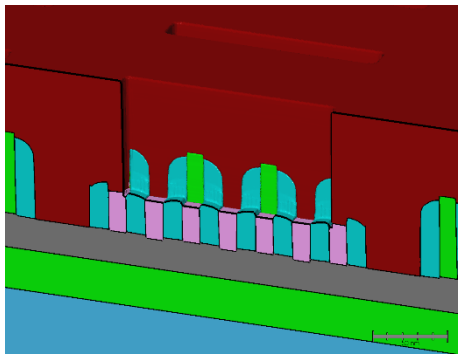
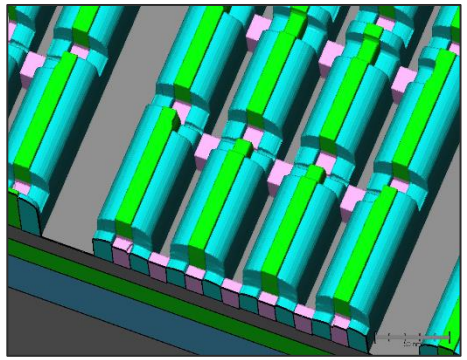


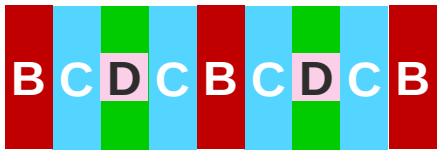
EPE tolerance in y-orientation = ¾ pitch

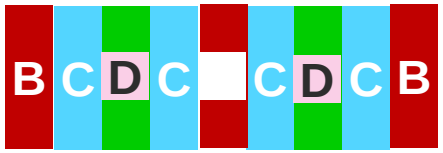
- **Utilize material difference in each metal track + etch selectivity to drive**
  - **Reduction in exposure passes → reduction in cost**
  - **Improved overlay tolerance in y-orientation**

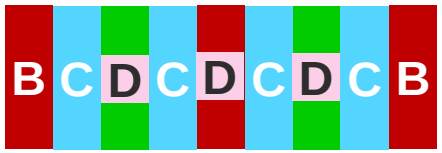
Spacer Side + Mandrel Side Plug Tone inversion small cuts

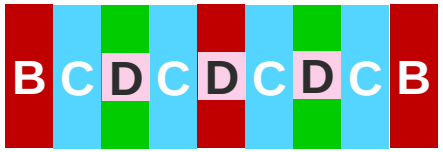
Cut “B” litho → SoC full open → SoG gap-fill 2 → SoG recess 2 → SoC ash

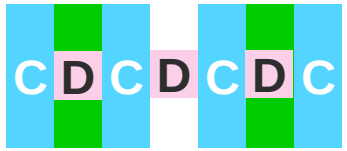








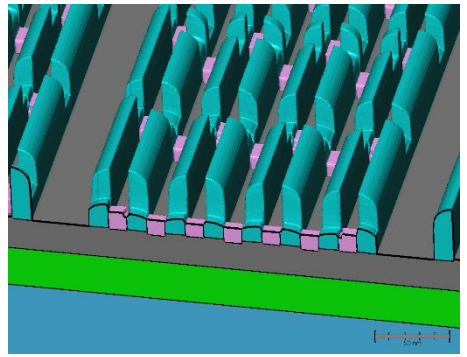
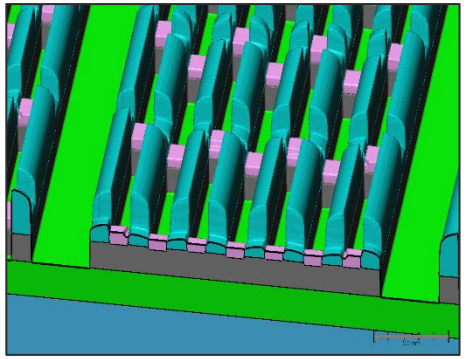
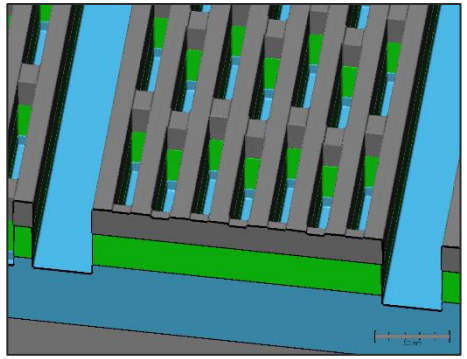
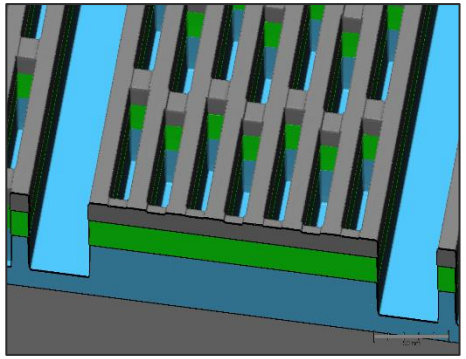
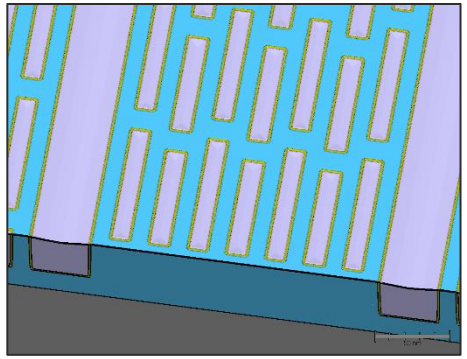


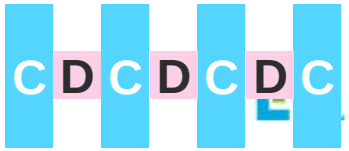


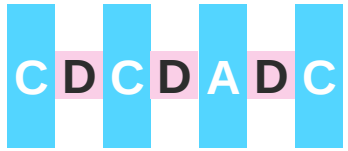


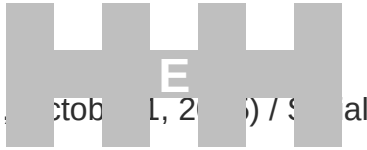


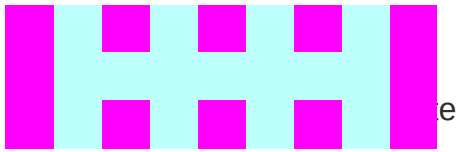
Mandrel pull → TiN transfer → SiN transfer → ULK transfer → Metal / CMP

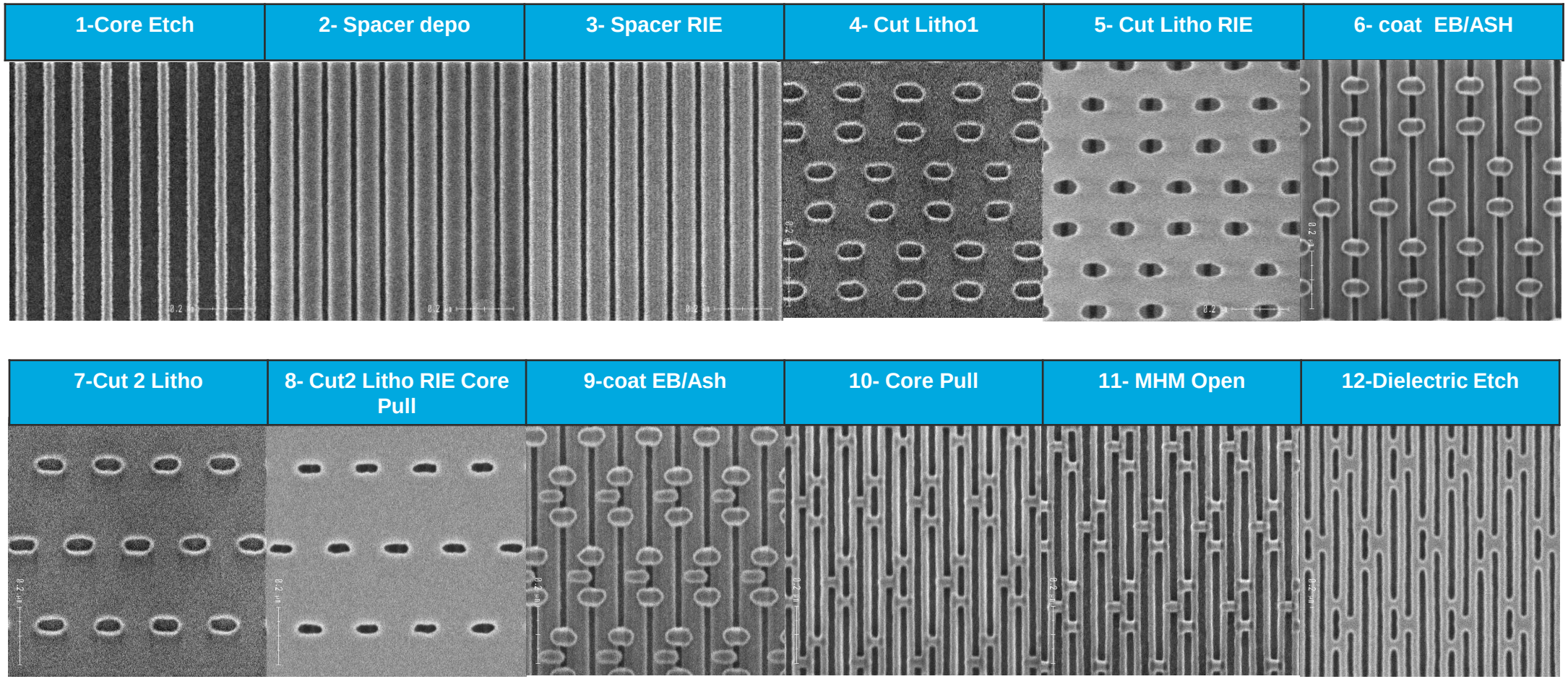








Spacer Side + Mandrel Side Plug Tone inversion small cuts



Complete SAB 2 cuts+ Spin on Block Tone Inversion for mandrel and non mandrel side demonstrated on silicon @50nm Pitch

Angelique Raley Self-Aligned Blocking Integration Demonstration for Critical sub 30nm pitch Mx Level Patterning with EUV self-aligned double patterning SPIE 2018

N3.2 - N3.3 - N14.7 – N22.64 (Node CD . Deck Scaling)

3D

Industry Devices Future : What will our *devices* look like?

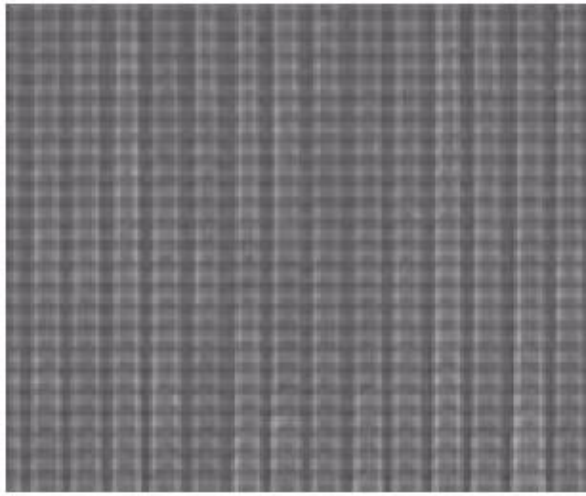
3D

Los Angeles = 2D

- Approach → grow while **squeezing** things **tighter**
- Industry unlikely able to extend beyond 20nm FINFET pitch
- EUV + multiple patterning very expensive for manufacturing

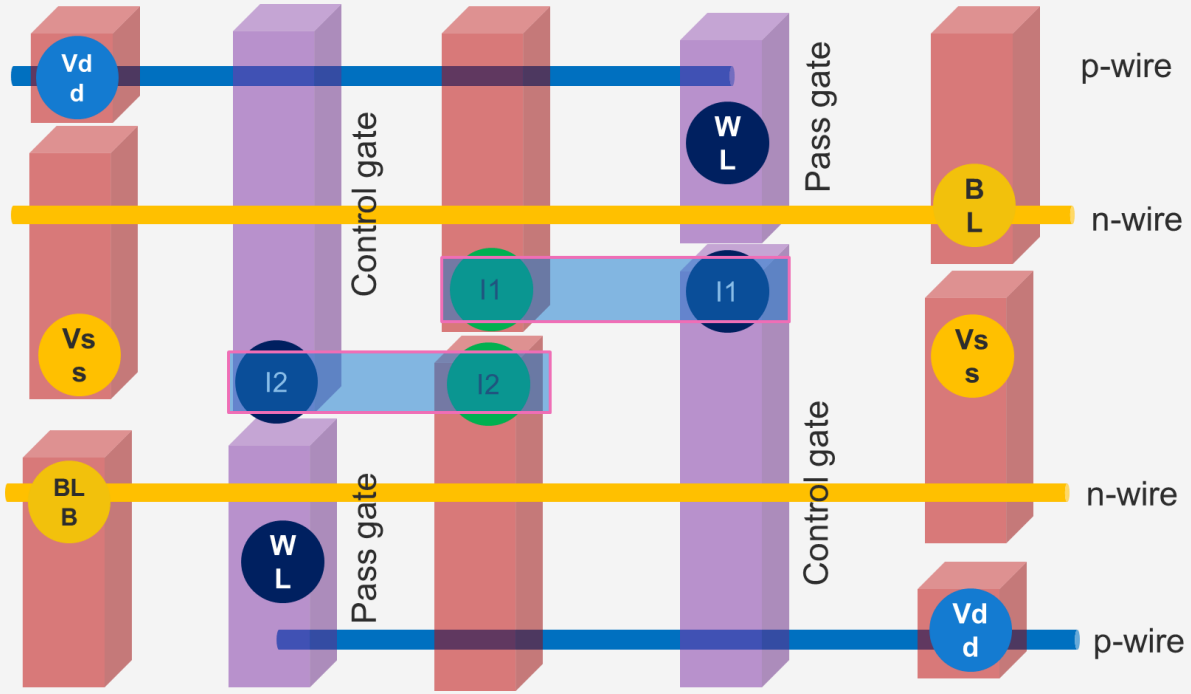
Tokyo = 3D

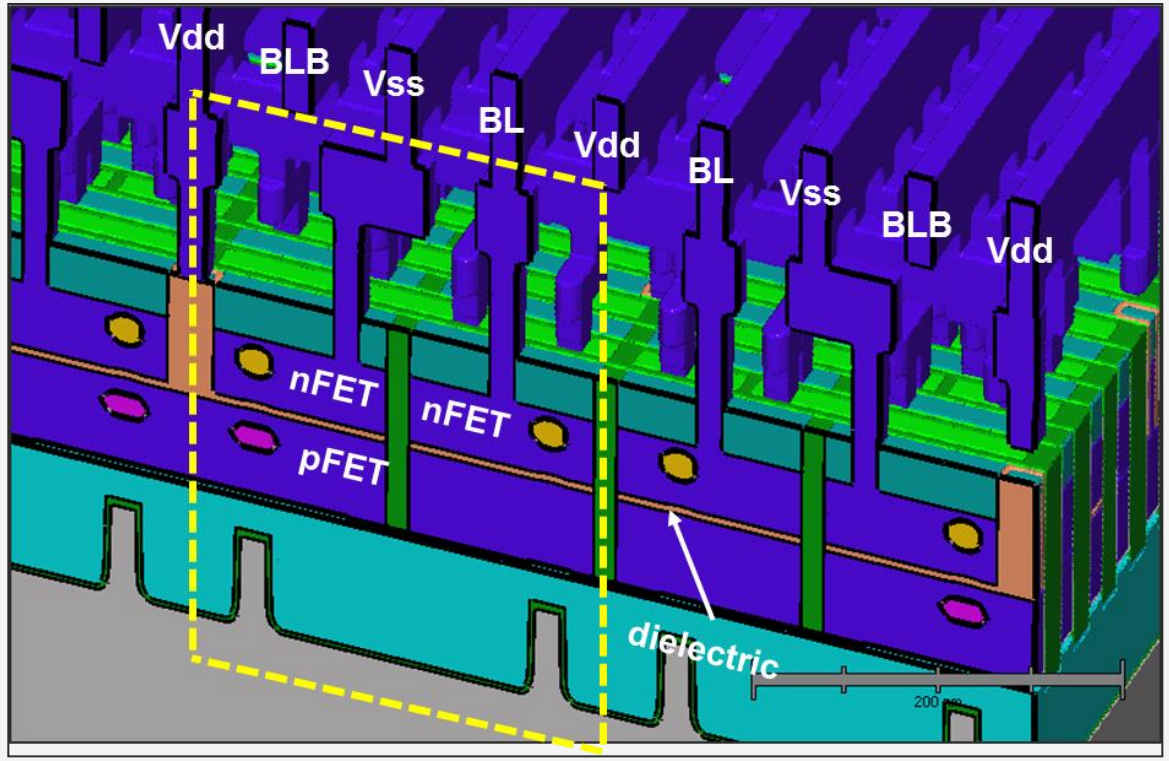
- Approach → grow while **building** things **higher**
- **3D logic** evolution is already here (FINFET → Nanowire → CFET)
- No need to extend beyond SAQP
- Further push-out of EUV?



Vertical NAND High Aspect Ratio

Early complimentary FET for SRAM device





Simple complimentary FET SRAM

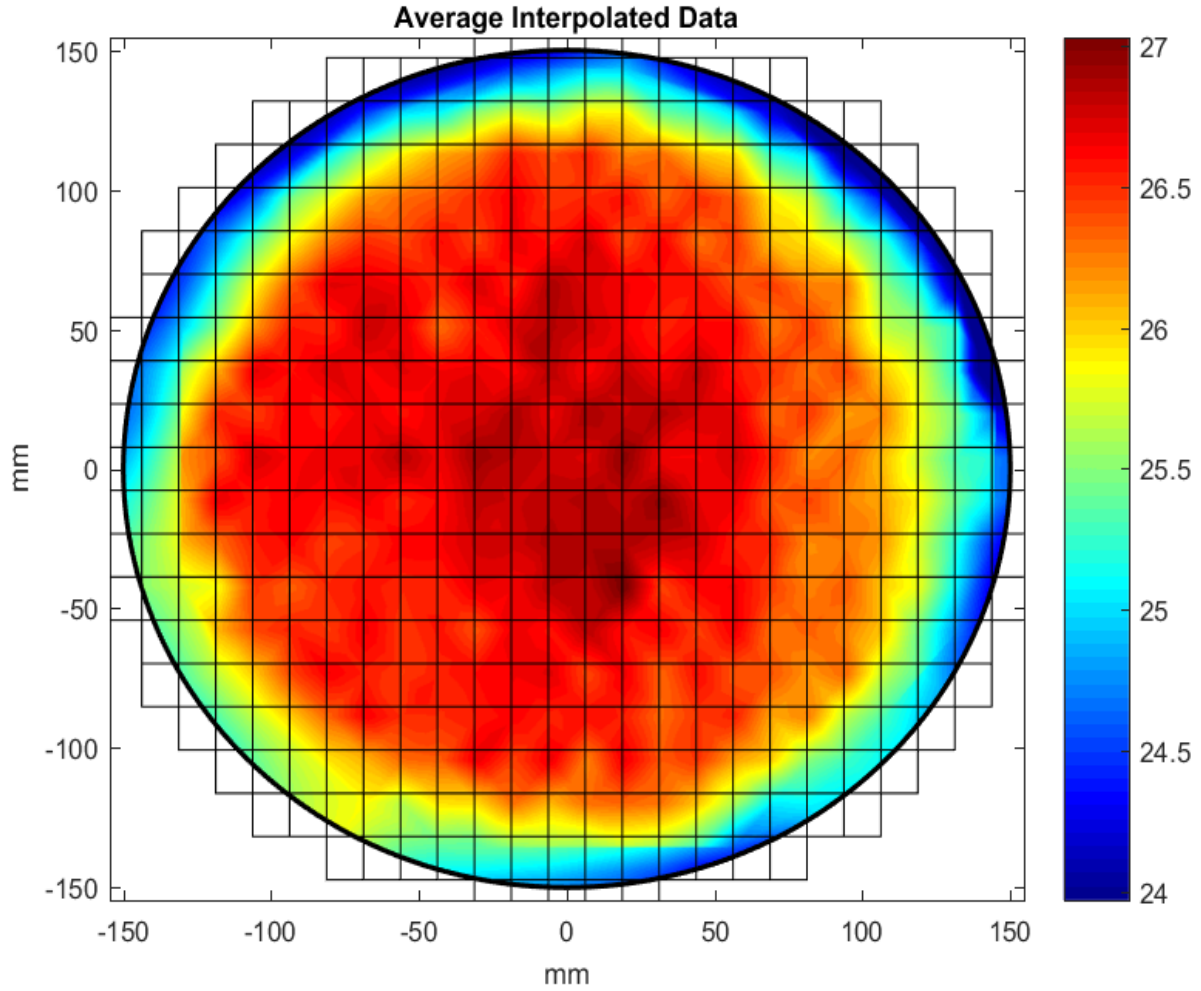
- ❑ nFET is stacked overtop pFET
- ❑ Nanowires allow pass and control gates to be side-by-side
- ❑ S/D bars can be “cut” to have separate connection to BL / Vss / Vdd

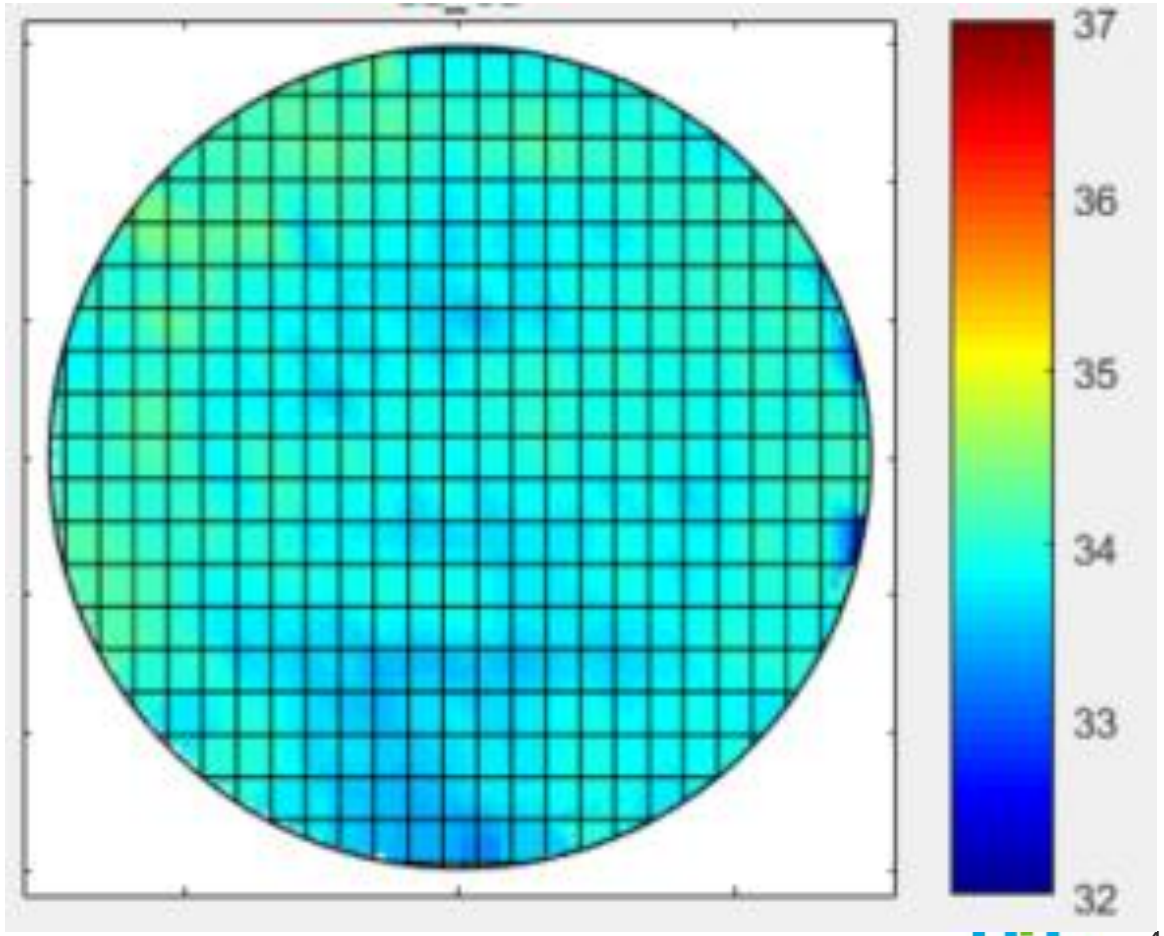
- ❑ SRAM cell size can fit within 4 total tracks @ M2

ETCH: Master ANY CD that came from a photo step with new Hardware ACDO – Used to solve Pitch Walking.

- Before pitch double core CD 2.13nm

After pitch double etch 0.59nm

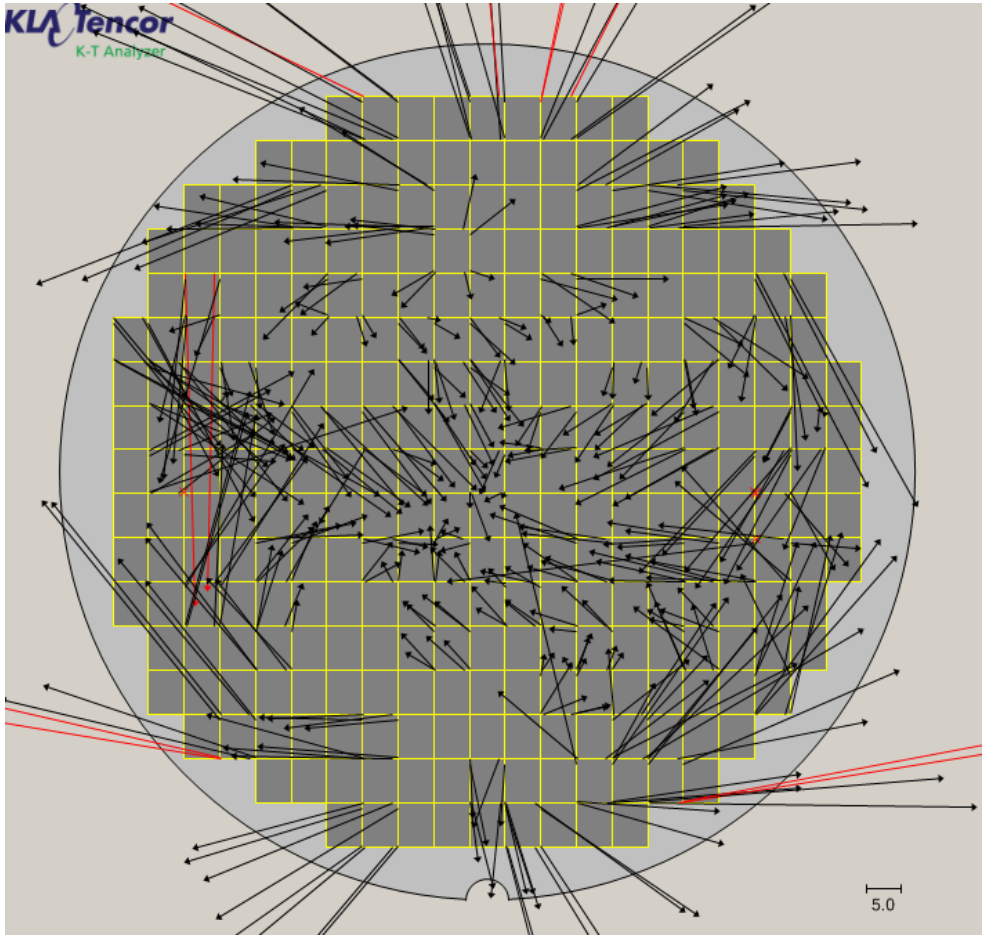




Master Overlay: Does Anybody have overlay bow Issues?

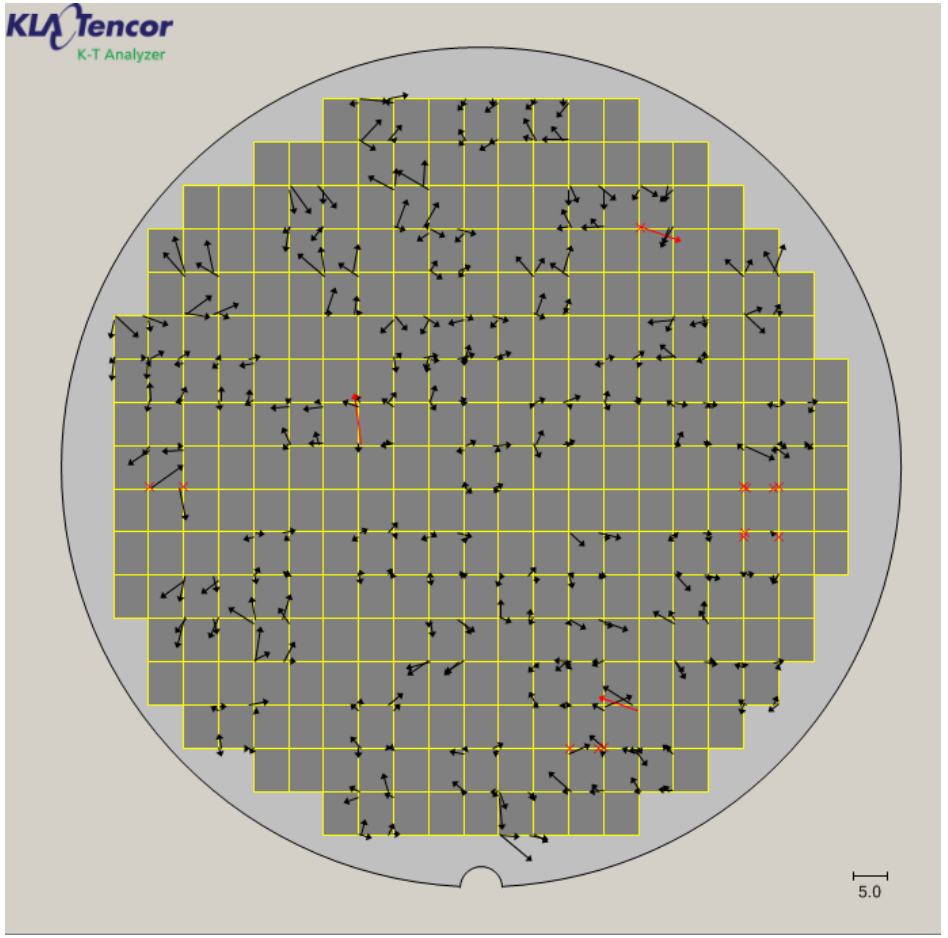
After warp, BEFORE bow correction

Test wafer created with Bow at TTCA – poor overlay

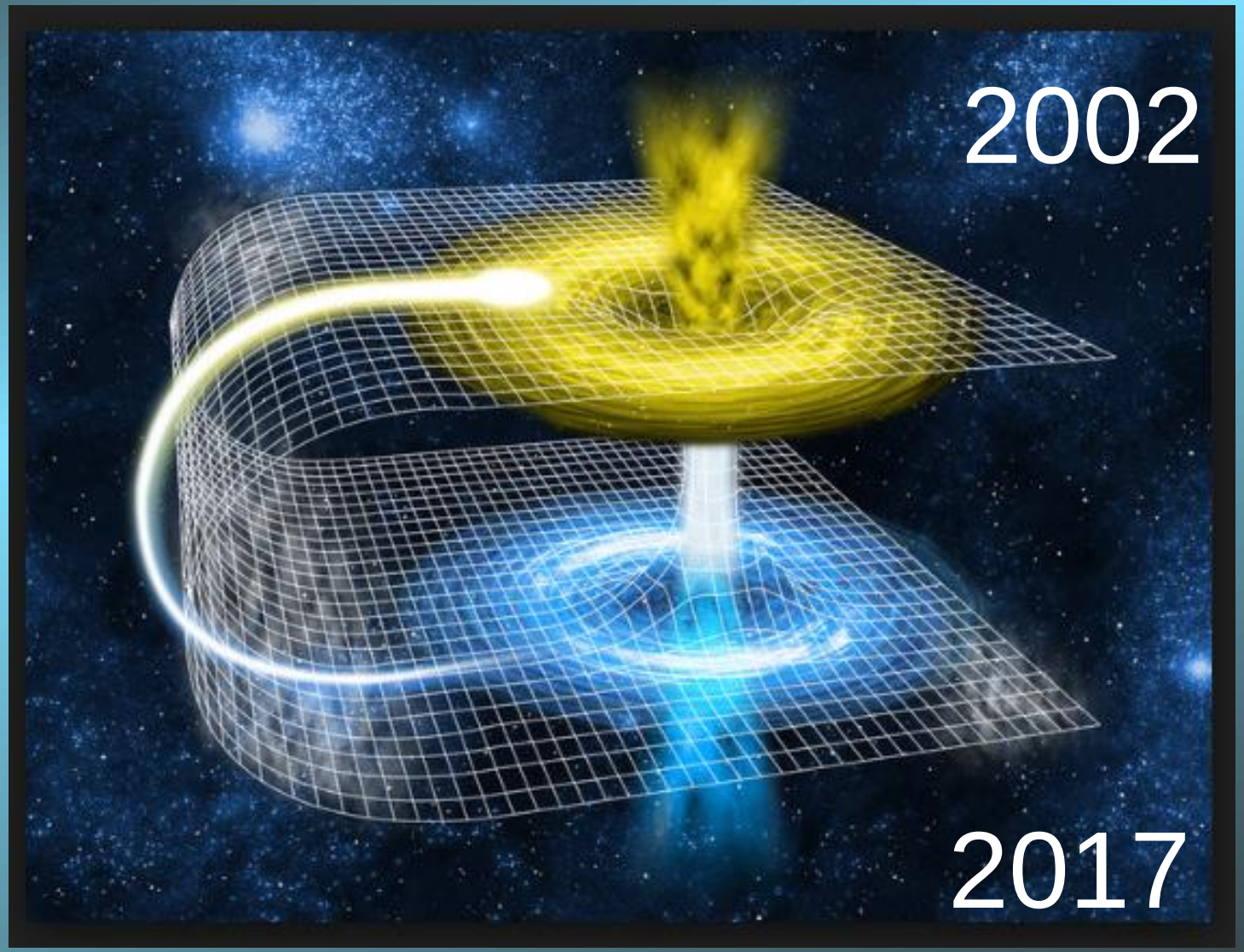


After warp, AFTER bow correction

Same wafer corrected – Awesome overlay



What would you tell yourself 15 years ago?



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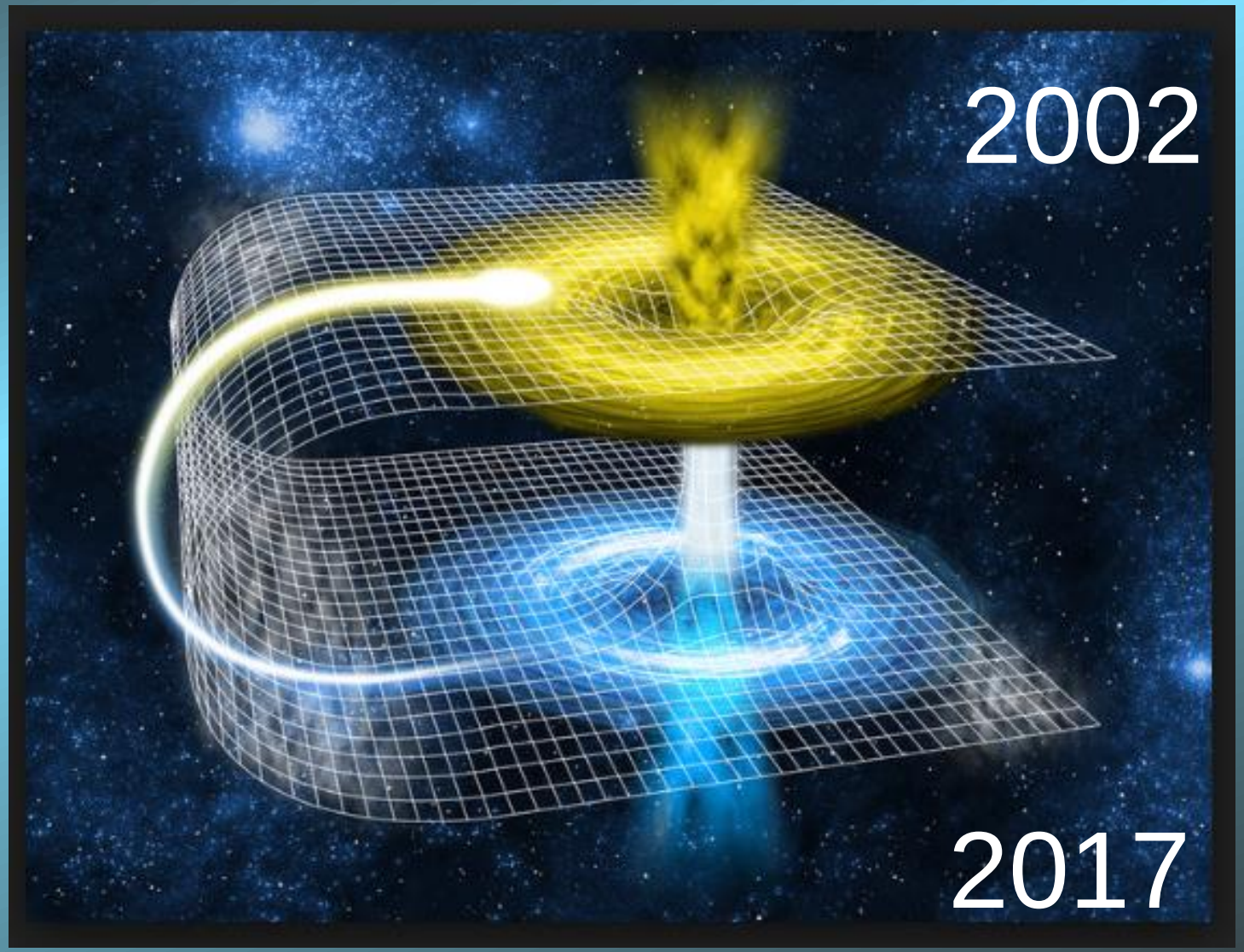
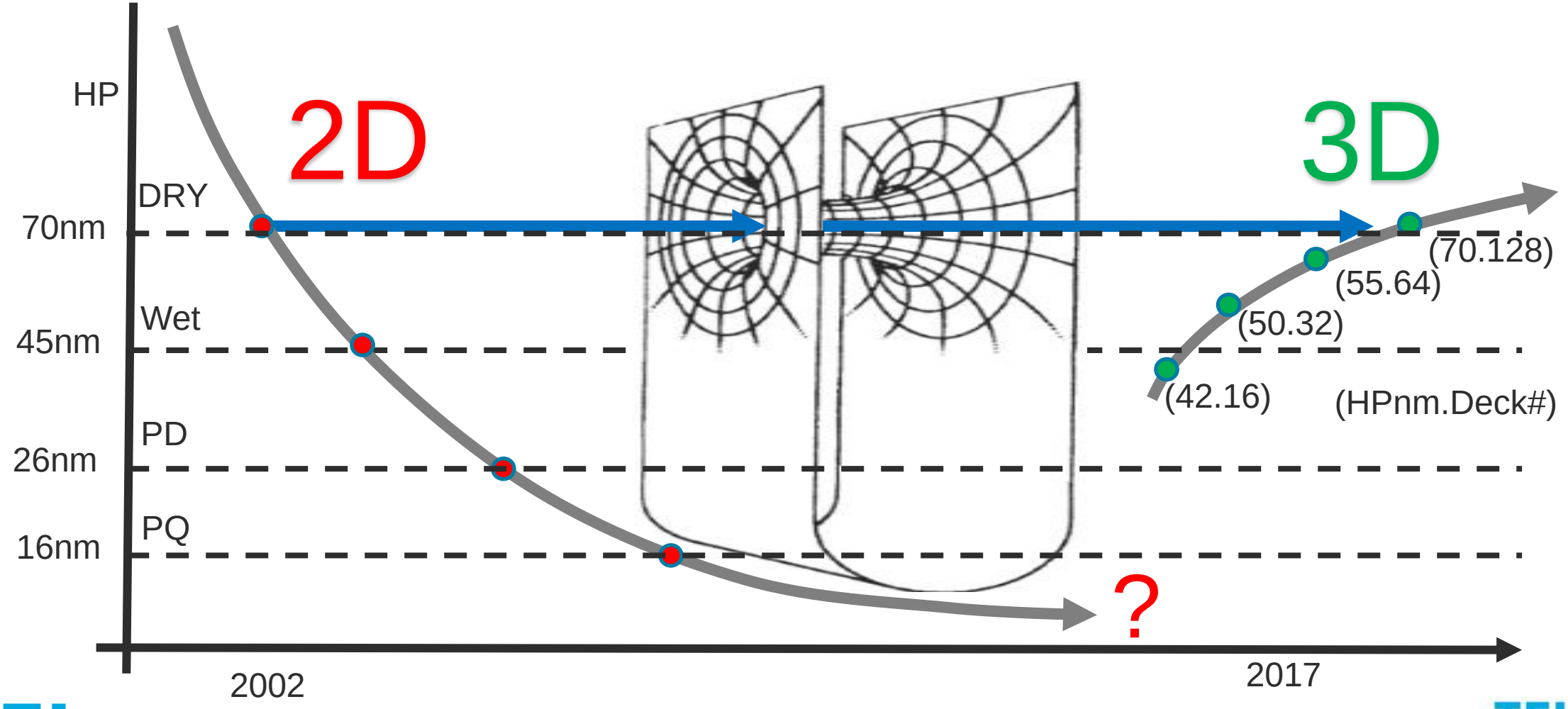


Other than Buy more TEL tools

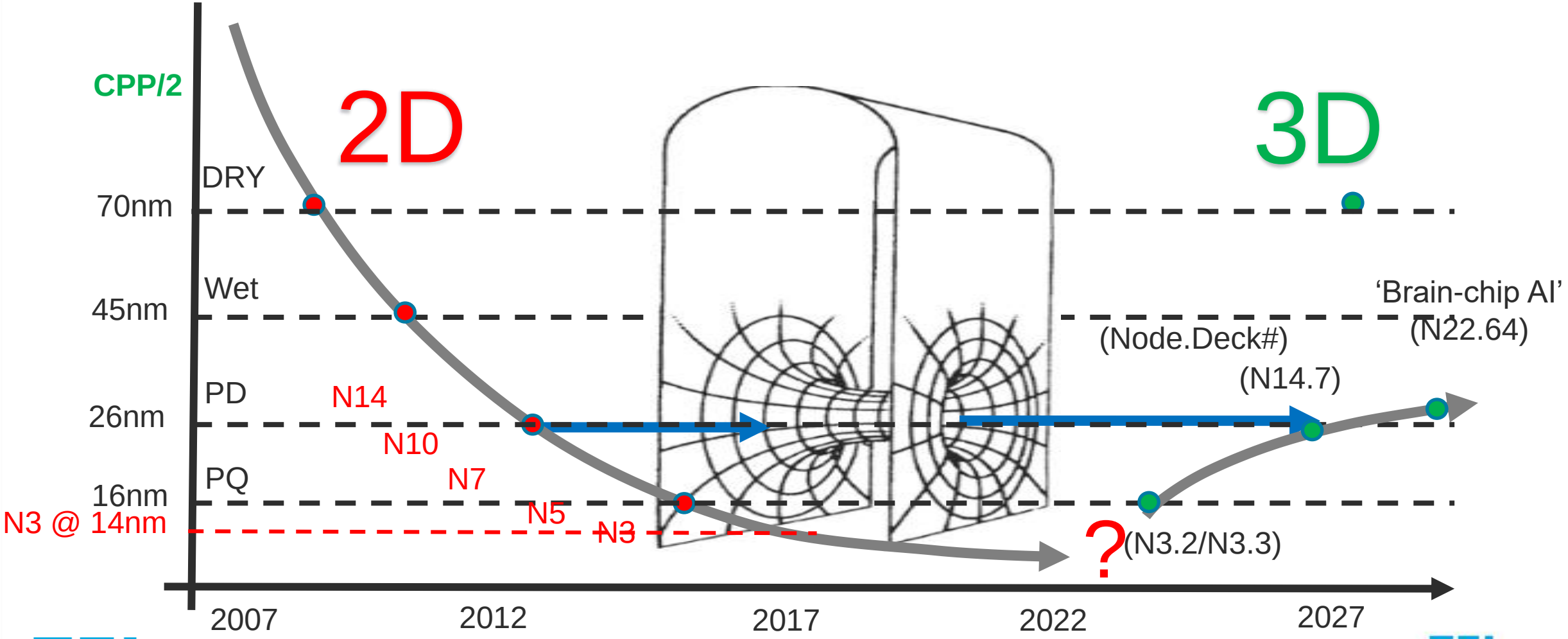
What happened in the history of memory scaling:

- Memory Half Pitch Scaling



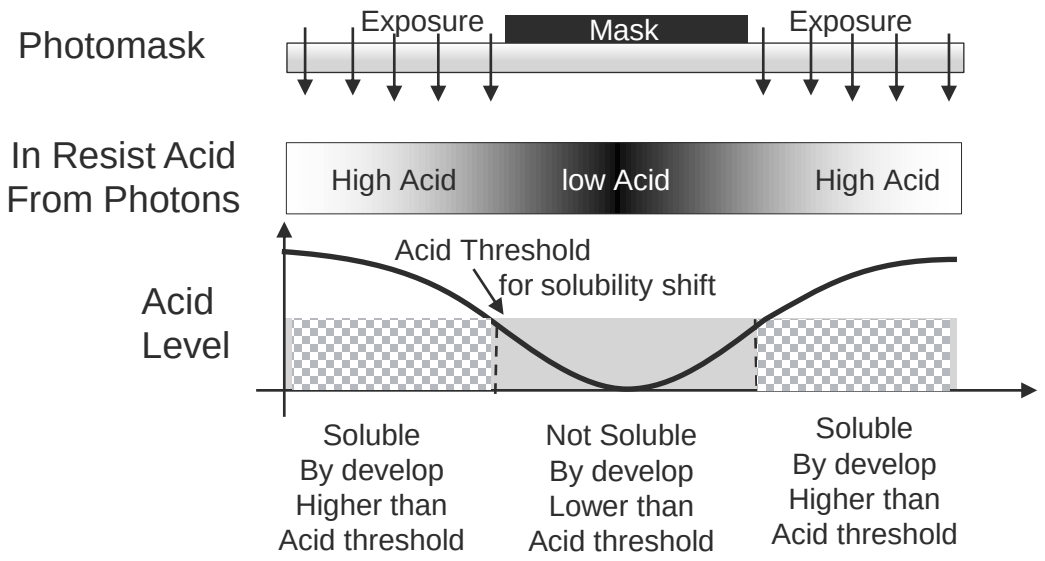
What might happen in the future of logic scaling:

- Memory Half Pitch Scaling



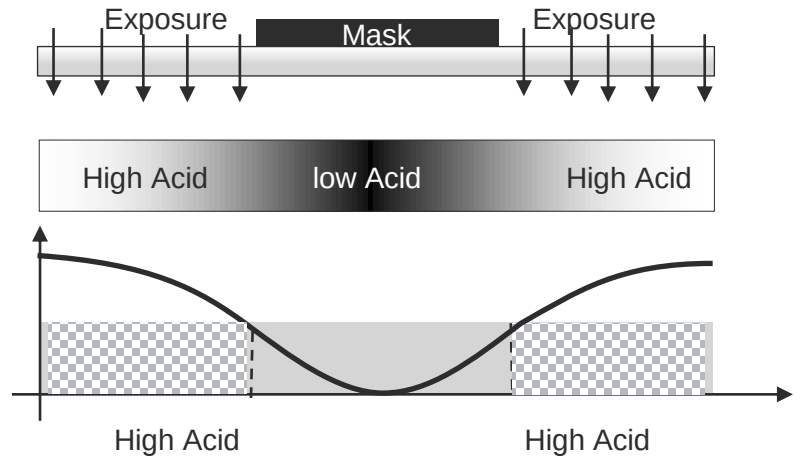
What is it ? Technology in a nutshell. All track Doubling

- How lithography works.



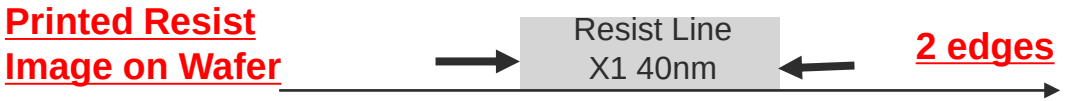
VS

- How Geminatio Works:



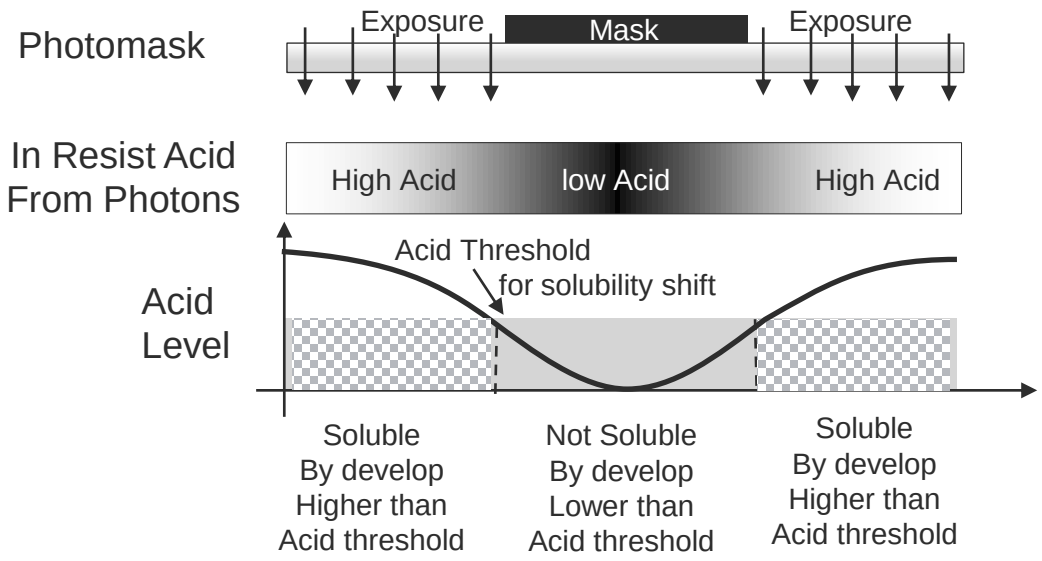
Exact Same till here
Then the Magic Happens

Mask creates 1X resolution copy at 1X Pitch



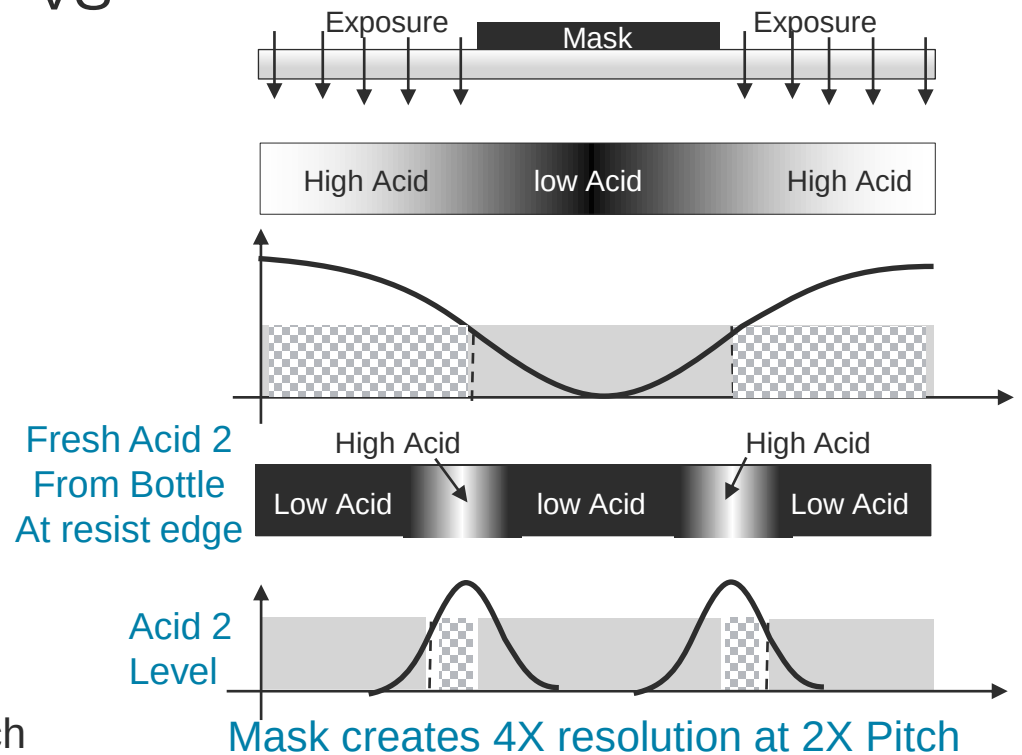
What is it ? Technology in a nutshell. All track Doubling

- How lithography works.



VS

- How Geminatio Works:



THREENEW MATERIALS INTRODUCED

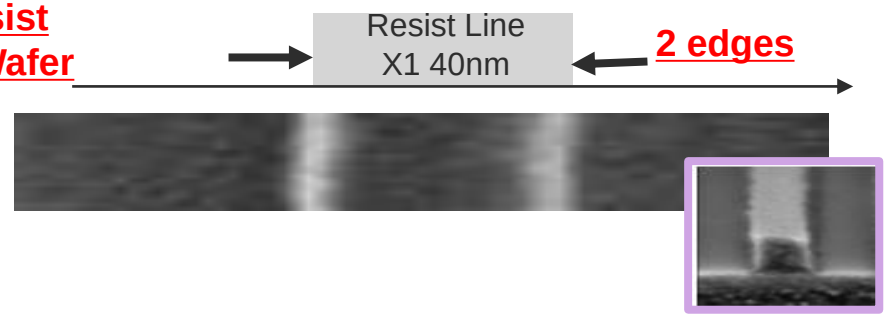
TRENCHER

MASKER

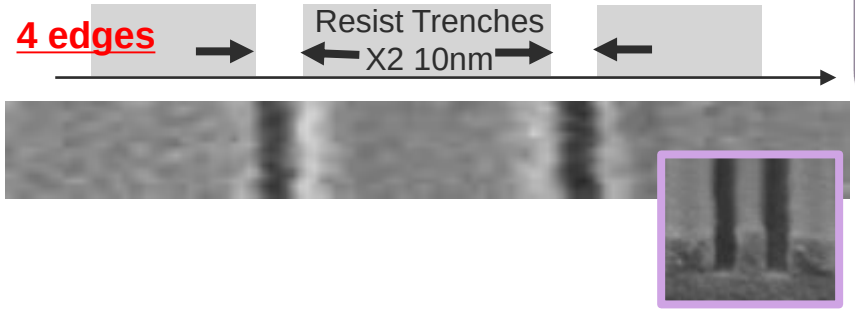
REMOVER

Mask creates 1X resolution copy at 1X Pitch

Printed Resist Image on Wafer



Mask creates 4X resolution at 2X Pitch

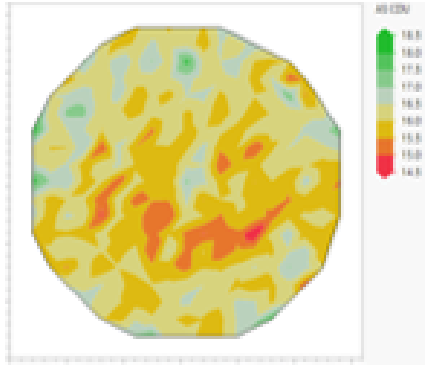


Anti-spacer “Black Arrow” Characterization

ArFi

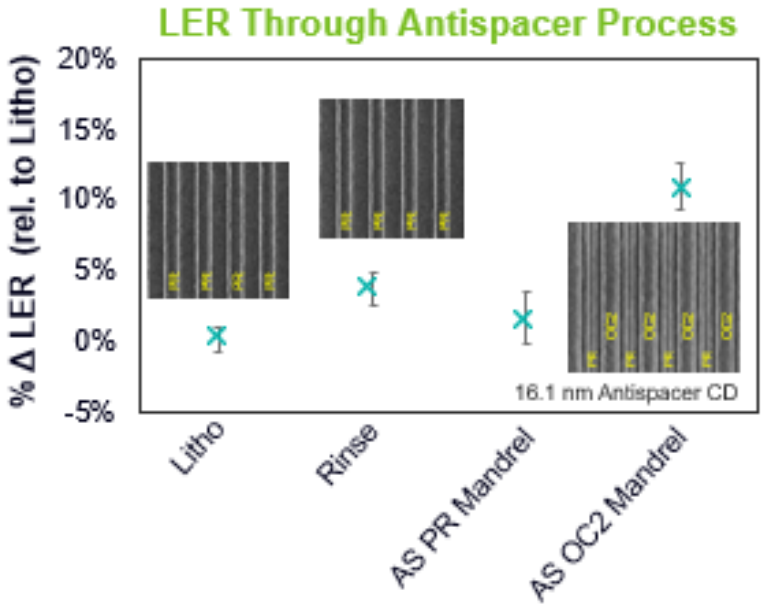
- CDU & LER Baselining

Antispacer Global Trench CDU



Mean Trench CD (nm)	Global Trench CDU 3σ (nm)
13.3	1.31 ± 0.11
15.6	1.68 ± 0.14
16.3	**1.60 ± 0.13**
20.0	2.09 ± 0.17
23.3	1.52 ± 0.13
26.9	1.66 ± 0.14

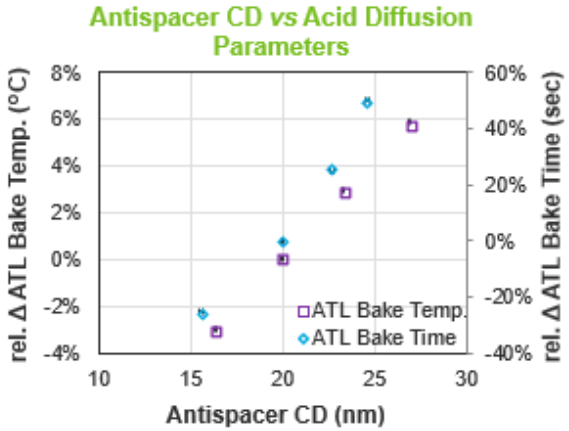
Based on 400 data points



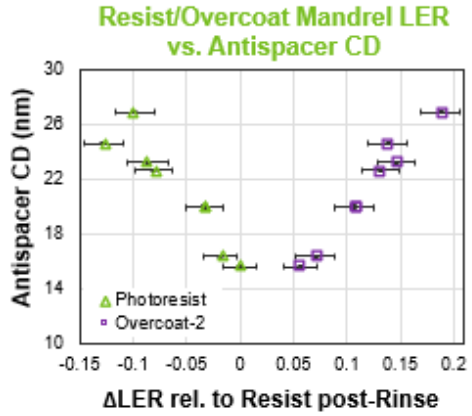
Anti-spacer “Black Arrow” Characterization

ArFi

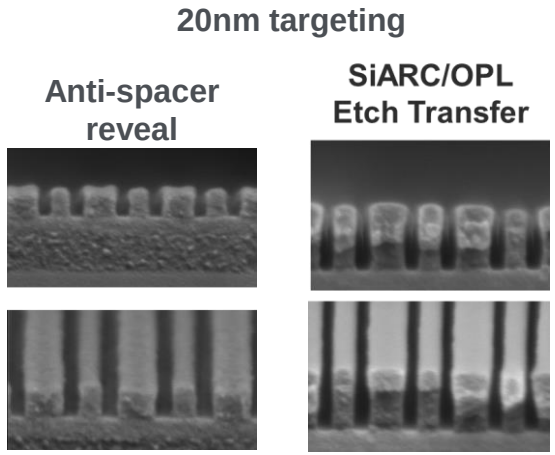
- Process windowing & initial HM transfer results



- Large CD process window achievable by variation in acid diffusion bake time and/or temperature
- Smaller CDs achievable at reduced resist film thickness

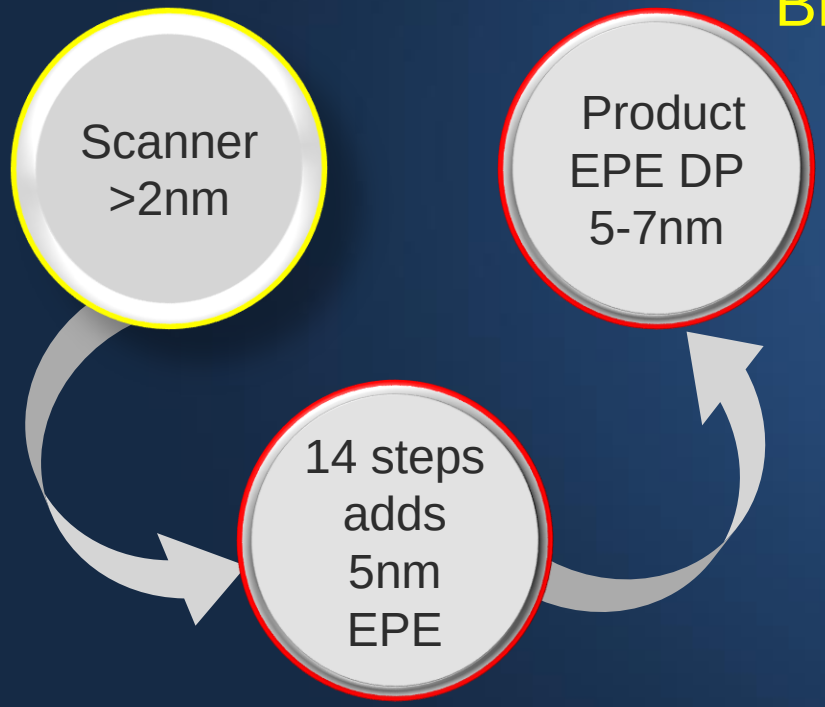


- Resist mandrel smoothed by acid diffusion front
- Overcoat mandrel roughened by TMAH recess
- Larger trench CD refreshes developer increasing LER

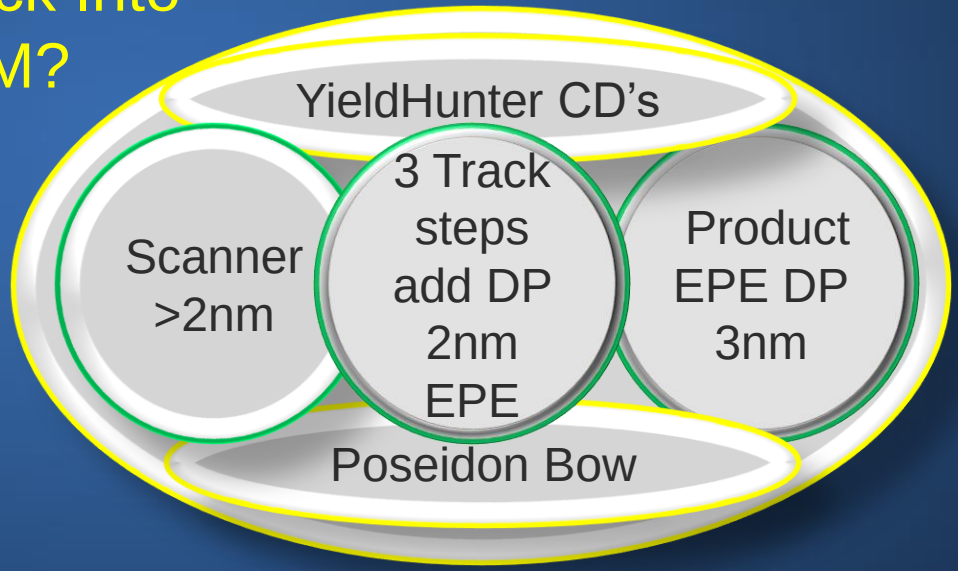


How Does DX change the game here and put litho back to the yellow room?

- ASML and TEL Eclipse our technologies together producing an all yellow room solution for double patterning and pitch splitting enabling litho based control.



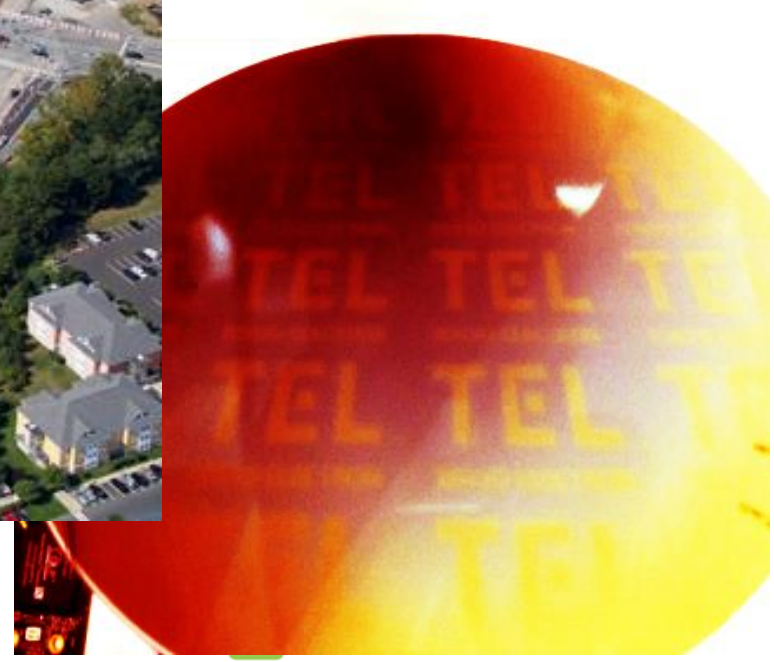
Bring everything back Into YELLOW ROOM?



With full digital transformation?

Acknowledgements

I wanted to acknowledge all members of Tokyo Electron Technology Center America, LLC for their support in this work and to all the many collaborators like IBM and throughout the industry.



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