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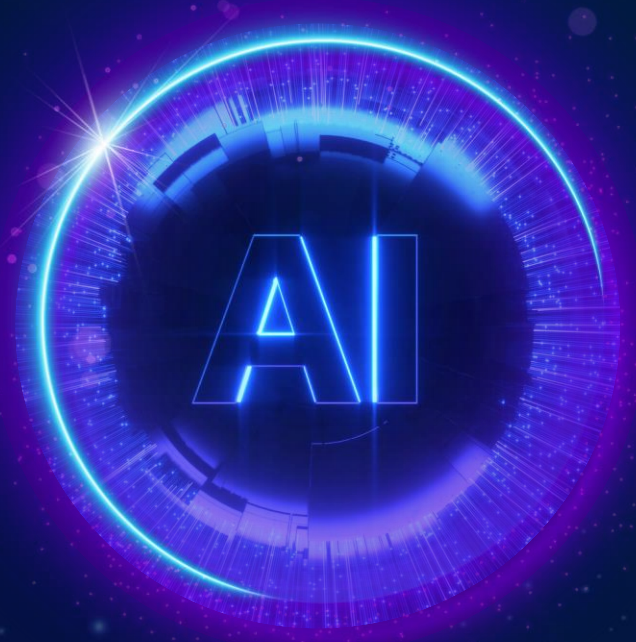
Artificial Intelligence
Executive Conference

explore the power of AI to transform semiconductor design & manufacturing



Presentation
Accelerating AI Skills Development

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01.

Situation & Challenges

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Situational Analysis

- Chips Act(s) are being enacted around the world bringing advanced manufacturing into new regions.
- Graduating engineers have very little training on IC manufacturing data
- Newly announced fabs are targeted to be foundries, handling many different chips instead of integrated device manufacturers (IDM) that build just a few chip designs
- Manufacturers internal systems and software are not modern nor applicable globally:
  - Many separate databases: All Silo’ed
  - 80% of engineers time spent on data wrangling
  - Require deep domain-specific knowledge
- Engineers need software manufacturing analytics tools and methods that enable them to be more productive at geographically distributed foundries

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Problem Statement

By 2030, 67,000 semiconductor positions risk going unfilled

39%
will require post-secondary certificates or two-year degrees

35%
will require four-year engineering or computer science degrees

26%
will require a masters or doctoral degree

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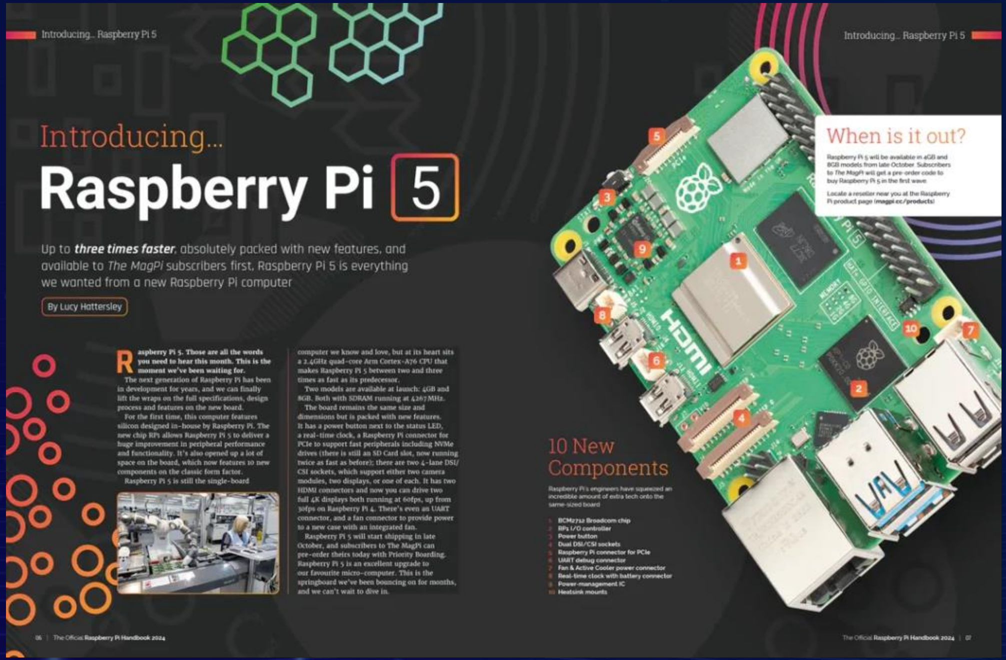
Challenge

University fabs focus almost entirely on hardware, with no connection to data infrastructure and limited access to software tools.

Digital twins require infrastructure to connect the hardware and software domains – now made easy with consumer-grade electronics.



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Challenge

CS majors focus almost entirely on software, without chip design, manufacturing, or other hard elements

Engineering programs are just beginning to emphasize big data, particularly as it relates to digital twins

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02.

First Implementation

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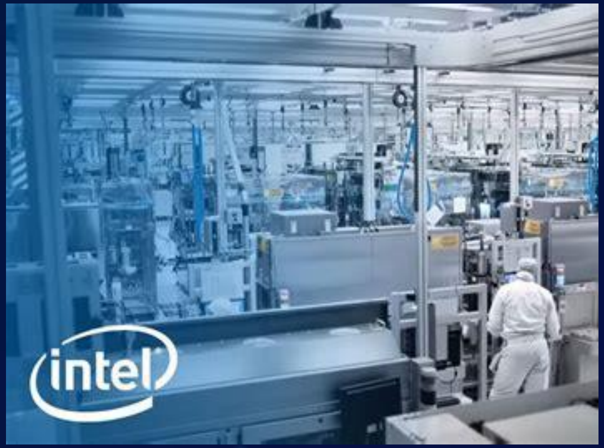
First Implementation: MS-Level Class at CMU

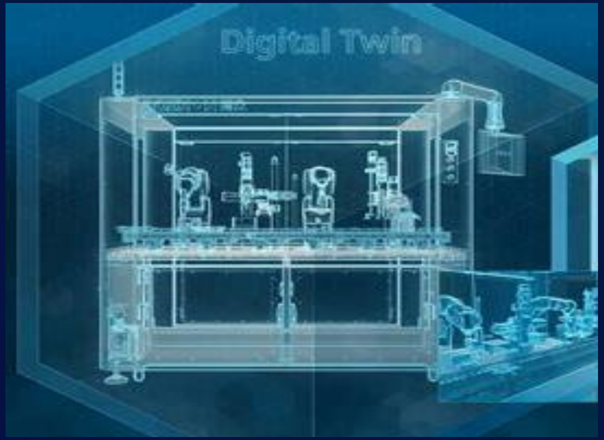
- Provide Exensio on the private AWS Cloud
- Create challenging use cases where students solve real problems in small teams
- Exensio data analytics deployed to arrive at solutions
  - The ML Modeling Pipeline is not provided to the students
  - Make the projects challenging
  - Promotes coming up with original creative solution
- ML model development for sanitized real data from PDF Solutions Virtual IDM and Intel
- Award the winning teams prizes ($500-1k)

First Implementation: MS-Level Class at CMU

- CMU customization:
  - Most MS students are already AI/ML savvy (either took the ML class or are taking it concurrently)
- However, weak semiconductor background
- Goal, while the focus is on ML, provide necessary backgrounds for the context:
  - Process Flow, Equipment, Device Architecture & Performance, SOC Components
  - Hardware for AI, Testing, Assembly including 3DHI
- Realistic Data Sets from Intel
- Intel participation: 3 Guest Lecturers
- **Many thanks to Dr. Sanjay Natarajan and his staff at Intel for their key contributions to the CMU course**

How students build the digital twins





Exensio AI Training Engine
Using the obfuscated data, the engine determines the significant parameters and wafer spatial distributions relevant to yield loss and test optimization.

Exensio AI Training Engine
Cross validate the model using different data sets.

Exensio AI Inference Engine
Apply the trained model to the real-life tasks.

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Project 2

- **Data set**: PDF's Virtual IDM based on historical data from an IDM customer
  - Fault Detection Classification (FDC) from the Scanner equipment, Trace data from the Anneal equipment, E-Test, Metrology and Wafer Sort Yield.
- **Goal**: identify the key FDC parameters causing the yield loss and IDDQ by performing root cause analysis and building predictive models for yield and IDDQ.
- Students really excited to work with real data
- They appreciate now how much the data pre-processing and datamining must happen before the ML model building to succeed

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Project 2 Insights

- The direct attempts to build the predictive models in ChatGPT failed to identify the key FDC indicators

- The winning approach:
  - Recognize that the yield losses were mostly at wafer edges by using Exensio's spatial (zonal) analysis
  - Spatial analysis on the Wafer Sort and Metrology data
  - Build hierarchical models (YAFDC methodology in Exensio): Metrology/Misalignment →Yield loss & IDDQ & FDC→ Metrology
  - The final stage is to build a predictive model for yield loss and IDDQ using built-in Exensio ML approaches that they learned in Project 1

- Make sure that the models are not overfitted by employing the appropriate training, testing and cross-validation methodology

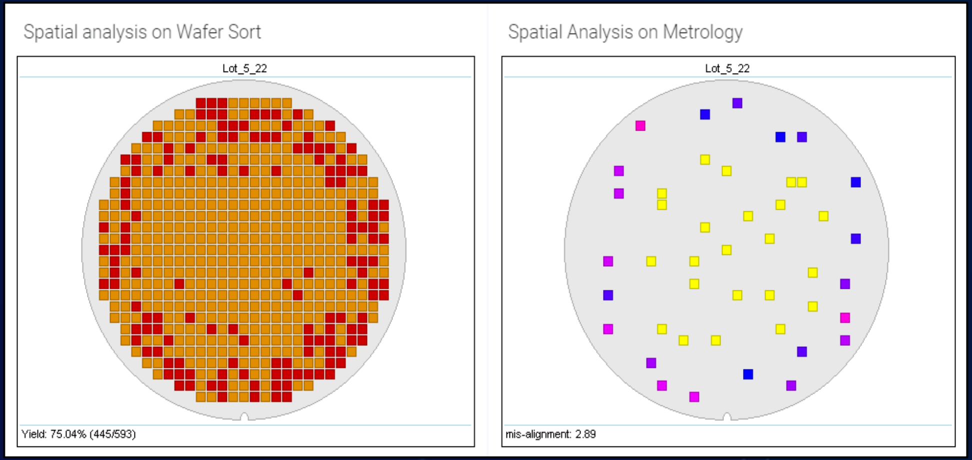

Figure 1 – Spatial Analysis on Wafer Sort and Metrology

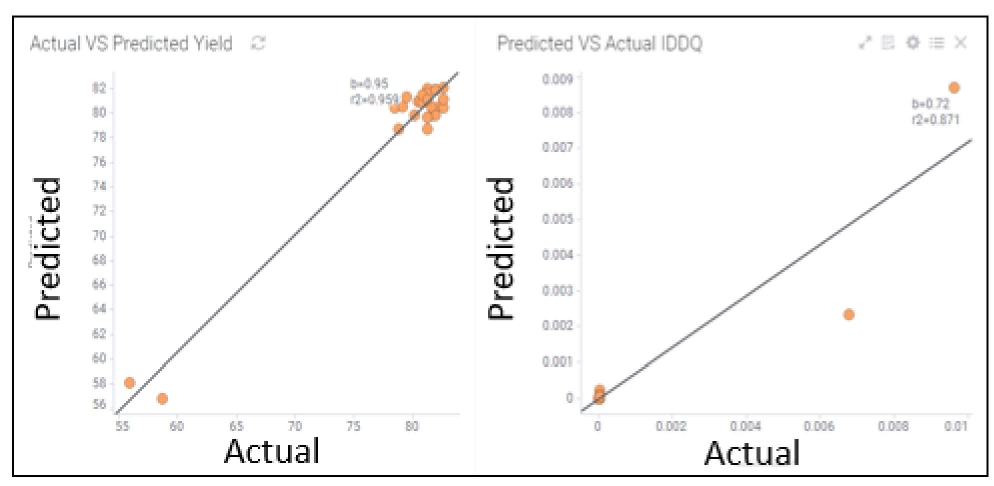

Figure 2 – Model Performance for Yield and IDDQ

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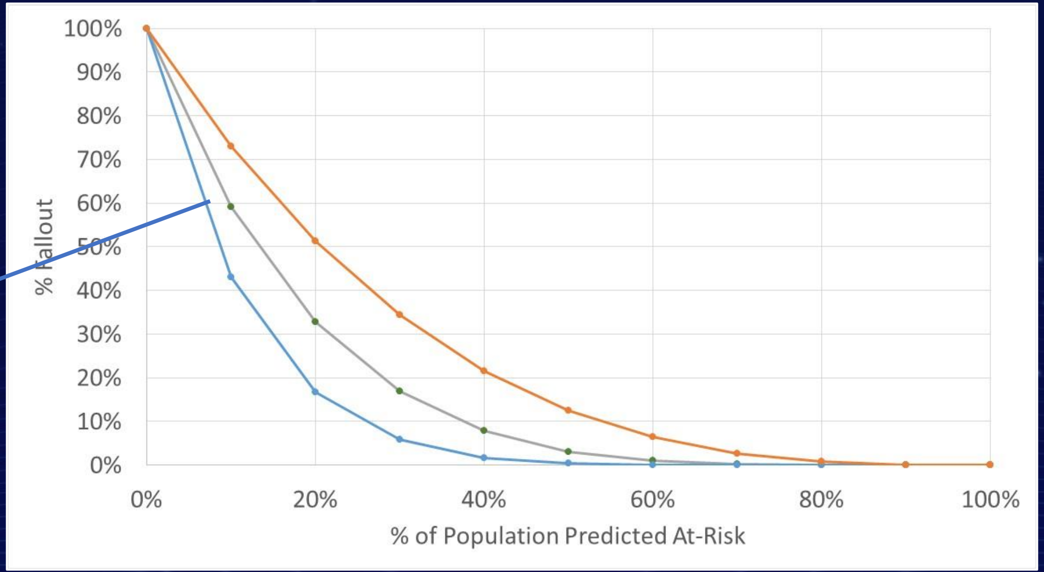
Project 4

- Intel data set: Sanitized data from a real product
  - This project involves data from the product which consists of two die in a package
  - Data set: Wafer Sort & Final (Class) Test data
- The primary objective to utilize ML Modeling Pipeline in Exensio for screening a vast dataset with 17k Wafer Sort parameters and 500k records (almost 200 GB of uncompressed data)
- Develop a predictive machine learning model for screening of die based on Wafer Sort test data to minimize the cost associated with assembling defective dies and rejecting the good ones.

Best Model



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Student Feedback

Exensio Feedback:

- Valuable datamining and pre-processing techniques
- Good applications of ML model development and validation
- Good support for screening, ML modeling and ANOVA
- Excellent visualization of data prep analytics and final results

Employment opportunities for the CMU MS students:

- 80% of students graduating in December 2023 went to semiconductor companies (all but one in US)
- PDF hired/or made internship offers to 25% of the class (including course TA)

03.

Further Plans

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Plans for the Analytics Courses

- Spring 2025: Second version of the CMU Course
  - Huge interest
  - Class size limit doubled compared to Fall 2023
  - ECE CMU juniors and seniors are eligible to take the course
  - More than 20 students on waitlist in the first 3 days of course registration
- Course can be expanded to more use cases contingent on available data sets. Participation opportunities for sponsoring companies
- Intel and PDF are planning to expand the class beyond CMU:
  - Arizona State, Ohio State, Internal class for employees for professional certificates
- Other US companies
- Oustide US
  - Germany
  - Japan: corporations
  - Taiwan: universities

Big Picture Goals

1

Develop workforce who can use software to bring to scale what has been done in conventional foundries w/ human capital

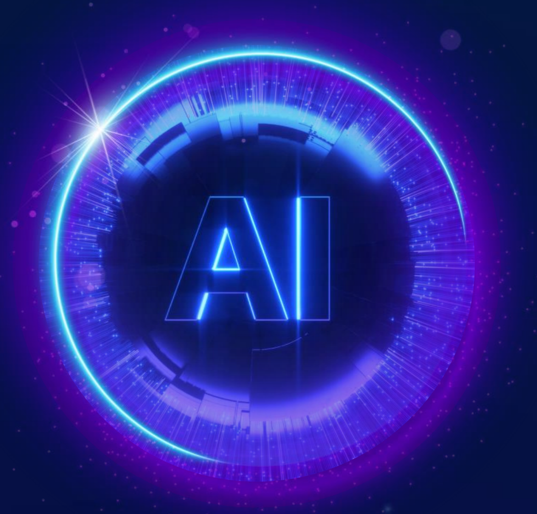
2

Develop a research community in the US that re-imagines analytics for fabs in the same way ad-tech was re-imagined

- Wide data (not just one tool or one equipment company)
- Real-time
- Personalized for each product

3

Scale US foundries, test and product engineering for the 21st Century



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