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2024 PDF Users Conference - China

Parkyard Hotel Shanghai – 669 Bibo Road, Shanghai, China, 201203

Automotive Solutions

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15th March 2024

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Automotive Market is growing fast

- **Increasing semiconductor percentage in cars**

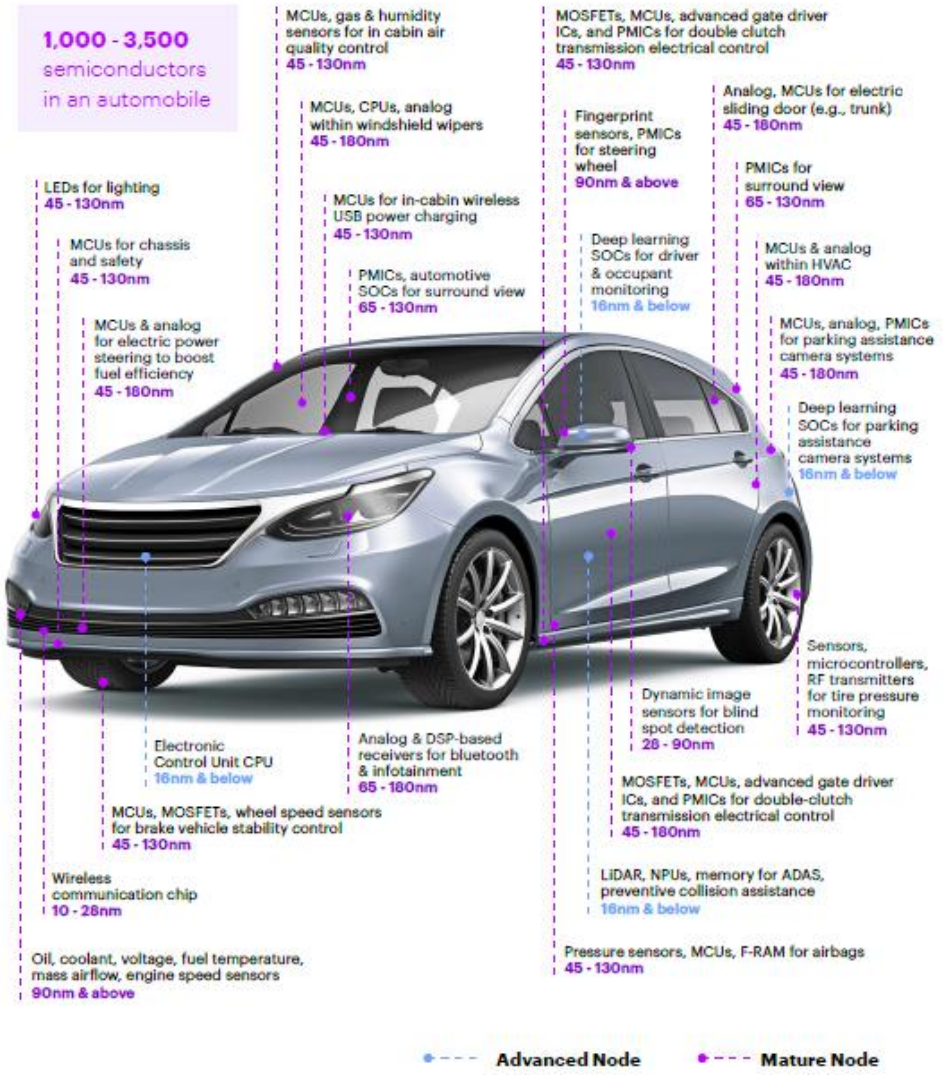
Exhibit 24: Semiconductor worldwide revenue by end vertical, sales (source: Gartner)

End vertical	Example	% of total 2020	% of total 2025E	2025 revenue projection	2021E-2025E% CAGR
Automotive	ADAS, Infotainment Chassis	8.3%	12.0%	$80.2B	12.4%
Communication	Smartphones	32.9%	31.5%	$210.3B	3.0%
Consumer	TVs, Digital Set-Top Box	10.4%	10.5%	$70.3B	2.6%
Data processing	PCs, Servers, Storage Media	37.7%	33.8%	$225.6B	1.6%
Industrial	Automation, Healthcare, Security	10.7%	12.1%	$80.7B	8.5%

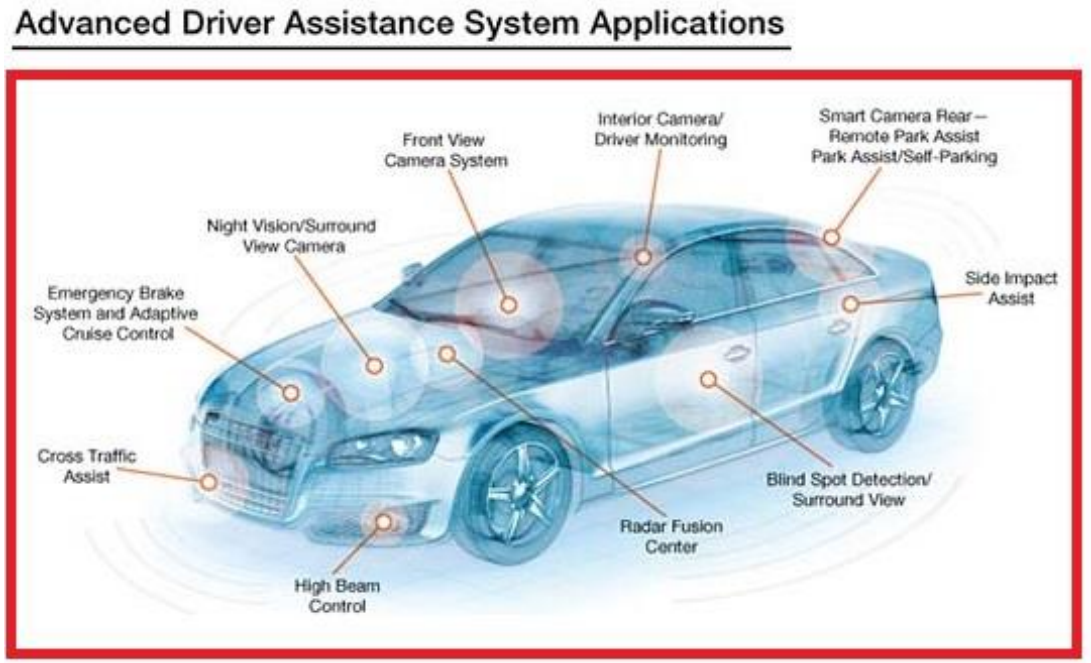
Overall Automotive 2025: 80B USD, 12.4% CAGR

Source: Accenture

Exhibit 34: Subset of advanced & mature nodes in an automobile



New technologies driving Automotive Market



Advanced Driver Assistance System Applications ~ NEW TECH (mytech2u.blogspot.com)

EVs

ADAS

Increased semiconductor percentage and complexity of the car

PDF Can Help You Succeed

- Solutions for Fabless
- Solutions for Foundries and IDMs
- Specialized solutions for Silicon Carbide

- Software
- Equipment
- Test Structures,
- & *Methodologies*

Health Check

Health Check: Basic and Advanced

- **What do we mean by basic & advanced?**
- **Basic = mature technologies**
  - Planar transistors ~22nm & above
  - Single die packages
- **Advanced = newer technologies**
  - 16nm FINFET & beyond
  - Multi-chip packages

- **Note: “Basic” in automotive does not mean *easy***

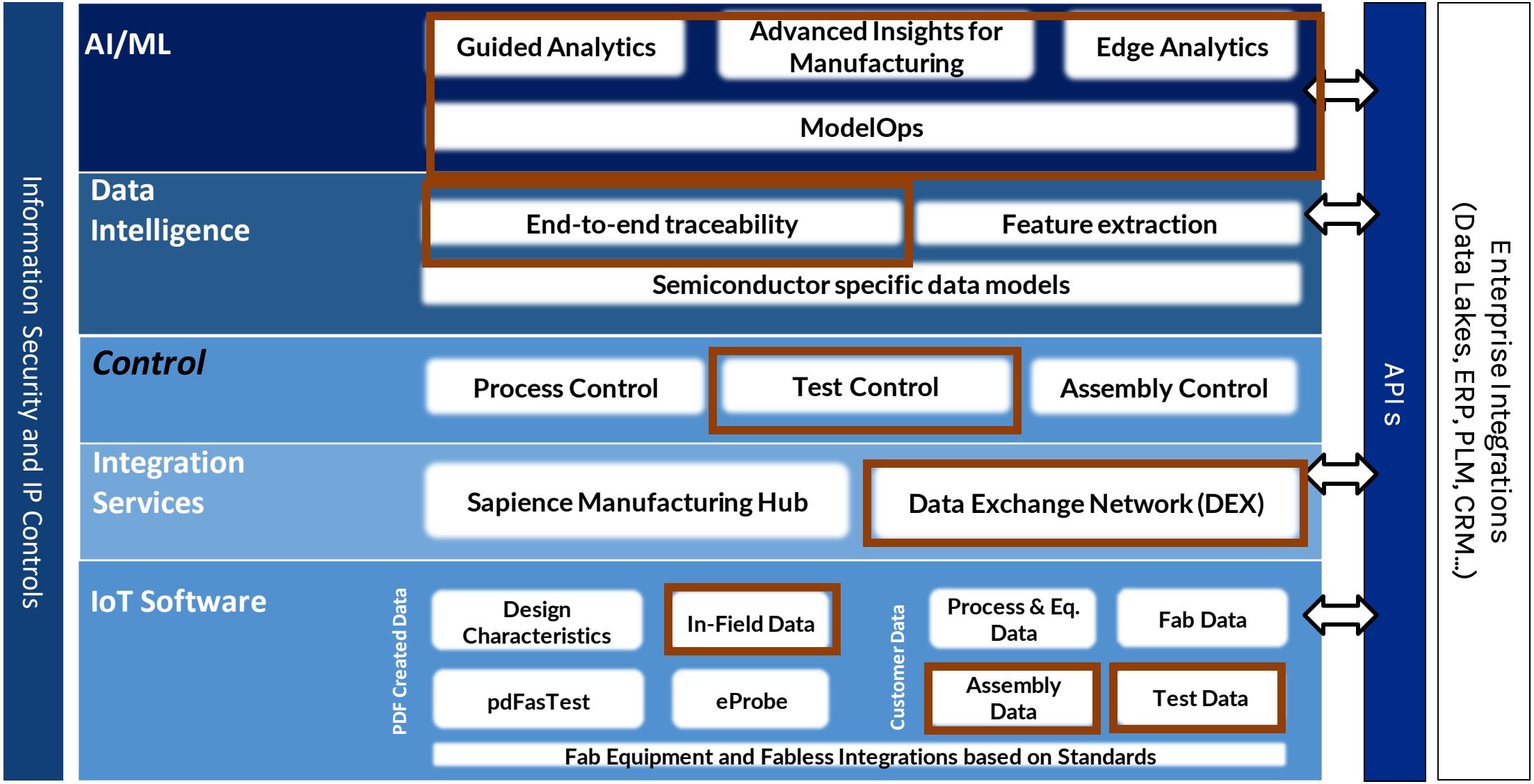
Health Check Results: Overall

Category	New Entrants		Incumbents		Best in Class Incumbents	
	Basic	Advanced	Basic	Advanced	Basic	Advanced
Design	69%	44%	86%	52%	95%	75%
Fab Mfg	59%	40%	92%	76%	100%	100%
Packaging	74%	65%	94%	88%	95%	100%
Test	71%	55%	74%	54%	95%	83%

- **Areas for Improvement – New Entrants**
  - Fault Coverage (!)
  - Pick the right Foundry if you are fabless
    - Regular layout
    - FDC with BIC control plans
    - Characterization Vehicles (CVs) for DFM
    - Margin WAT
- **Areas for Improvement – Achieving Best-in-Class**
  - Quality Shield
  - Adoption of traceability
  - Fault localization

Solutions for Silicon Devices

End-to-end Integrated Platform for Semiconductor Analytics



Silicon Product Lifecycle

Process Development	• Regular Layout • Characterization Vehicles
NPI/Char	• Characterization
Yield Ramp	• Accelerating Yield Analysis • Machine Learning for Optimized Test
HVM	• Best-in-Class Operations at Test • Supply Chain Visibility & Security
In-Field	• Failure Analysis & Returns

Process Development Phase

Make the Process Right EARLY

- **Build on a solid foundation**
- **Fix the problems early in the process**
- **Don’t wait for Test and hope to screen**
- **Test will miss things**

- **Early means *both***
  - Early in the development cycle
  - And
  - Early in the process flow

Be the right fab / Pick the right fab

- *What the customer wants*
- Superior yield
- Excellent process control
- Fewer excursions

- *How to get it*
- Regular layout
- Characterization Vehicles (CVs) for DFM
- Margin WAT
- FDC with BIC control plans

For Foundry & IDM
Be the right fab

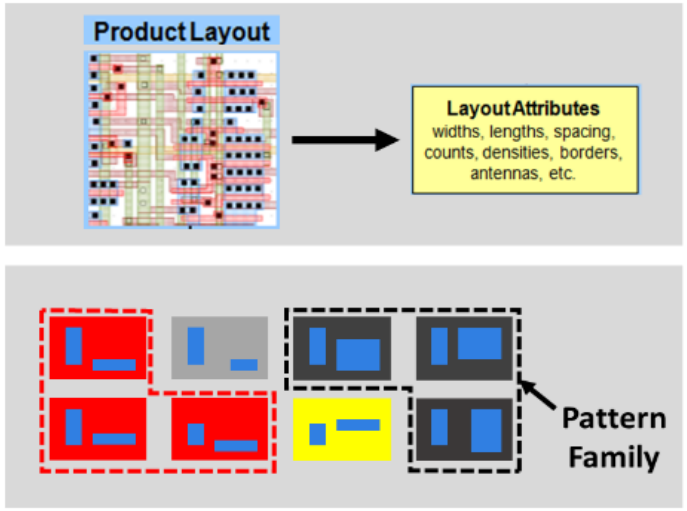
- *How to get it*
- Pick the right foundry
- One that uses these methodologies

For Fabless
Pick the right fab

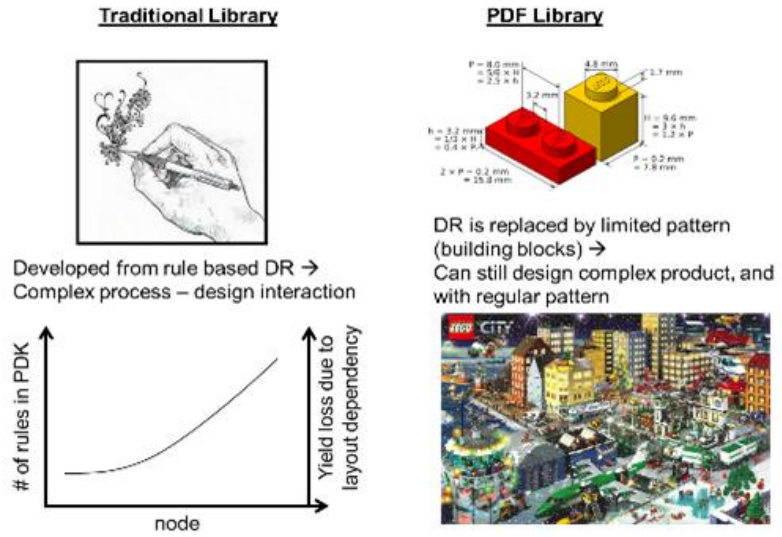
Design to Enable Zero Defect

Identify and Reduce Layout dependency

FIRE: identify all layout patterns in design



Templatyzer: reduce library pattern count by 10X

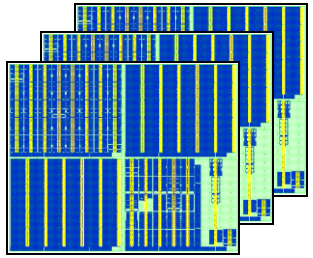


FIRE/Templatyzer for right-first-time

Regular Layout

- More consistent yield
- = fewer outliers
- = fewer excursions
- = lower defects

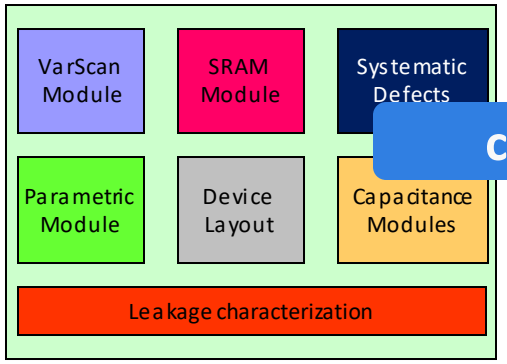
Characterization Vehicles & Test Structures



CV® test chips

Pre-PDK Early TD/TD → NPI → Ramp → Mass Production → foundry

NPI → Mass Production → fabless



content

Design and Process Co-optimization

Product Yield Ramp

Production Stability

Process & Recipe tuning
Weak pattern & hot spot
Model Validation
Failure mode detection

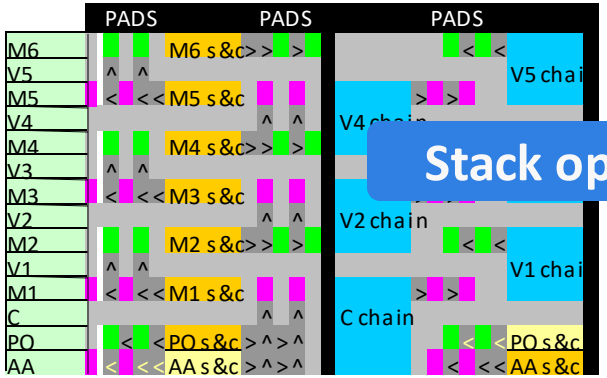
Health of Line examination
CPL matching
Yield diagnosis and ramp
Wafer edge improvement

IDU improvement and
Variation reduction
Excursion monitor and
prevention

Shared Reticle CV

DPCV

Scribeline CV



Stack option

Not just test chips, but methodologies

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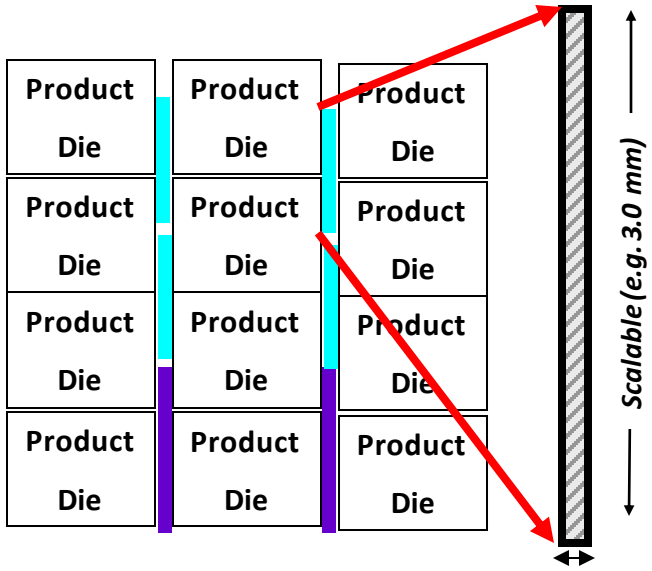
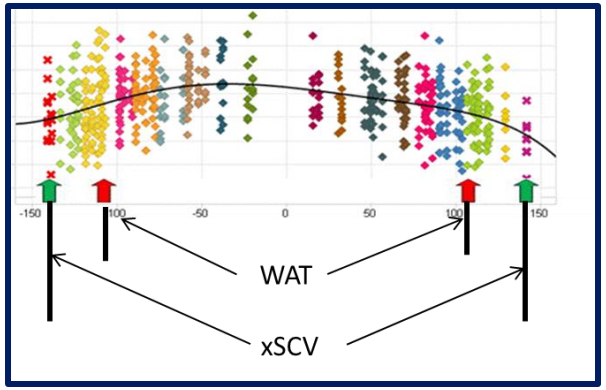
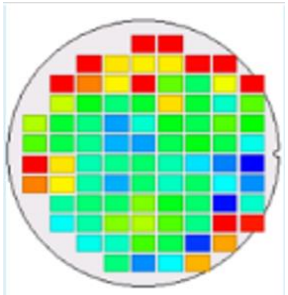
ScribeCV – PDF's Solution for Margin WAT



5th generation
pdFasTest-F380+
256 dual port channel arch.
High V & pulse generation



Yield learning & monitor wider wafer coverage



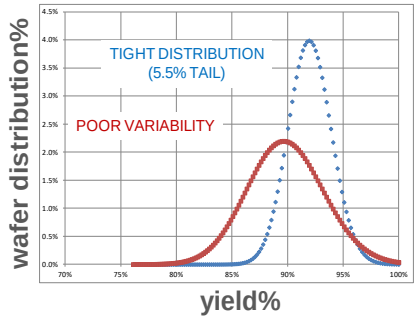
Scribe CV®

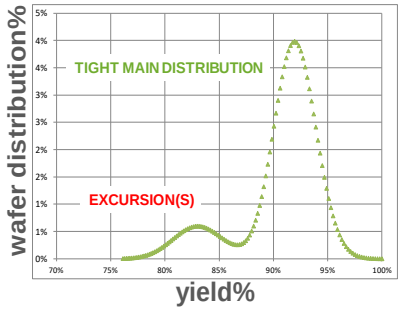
Device, Yield, Parametric, Leakage

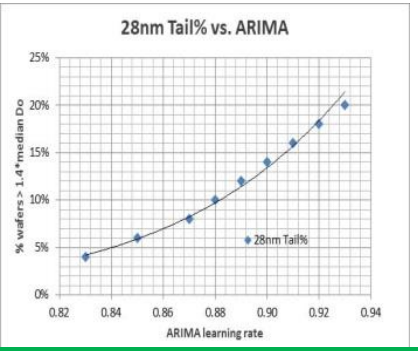
Process Control: Advanced FDC for Semi Manufacturing

All semi data managed in one location and built on Cassandra/Spark/R Big Data Platform

- Industry leading Advanced FDC control
  - Over 40,000 process tools under PDF control at foundries & IDMs
  - Online control and offline analytics
  - Advanced analysis, AI, ML, SPC, OCAP, dashboards, automation
- Enables FDC based decisions and process control at tool and factory levels:
  - Reduced excursions & tool induced process variability
  - Reduced maintenance resource costs and requirements
  - Tighter yield and parametric distributions







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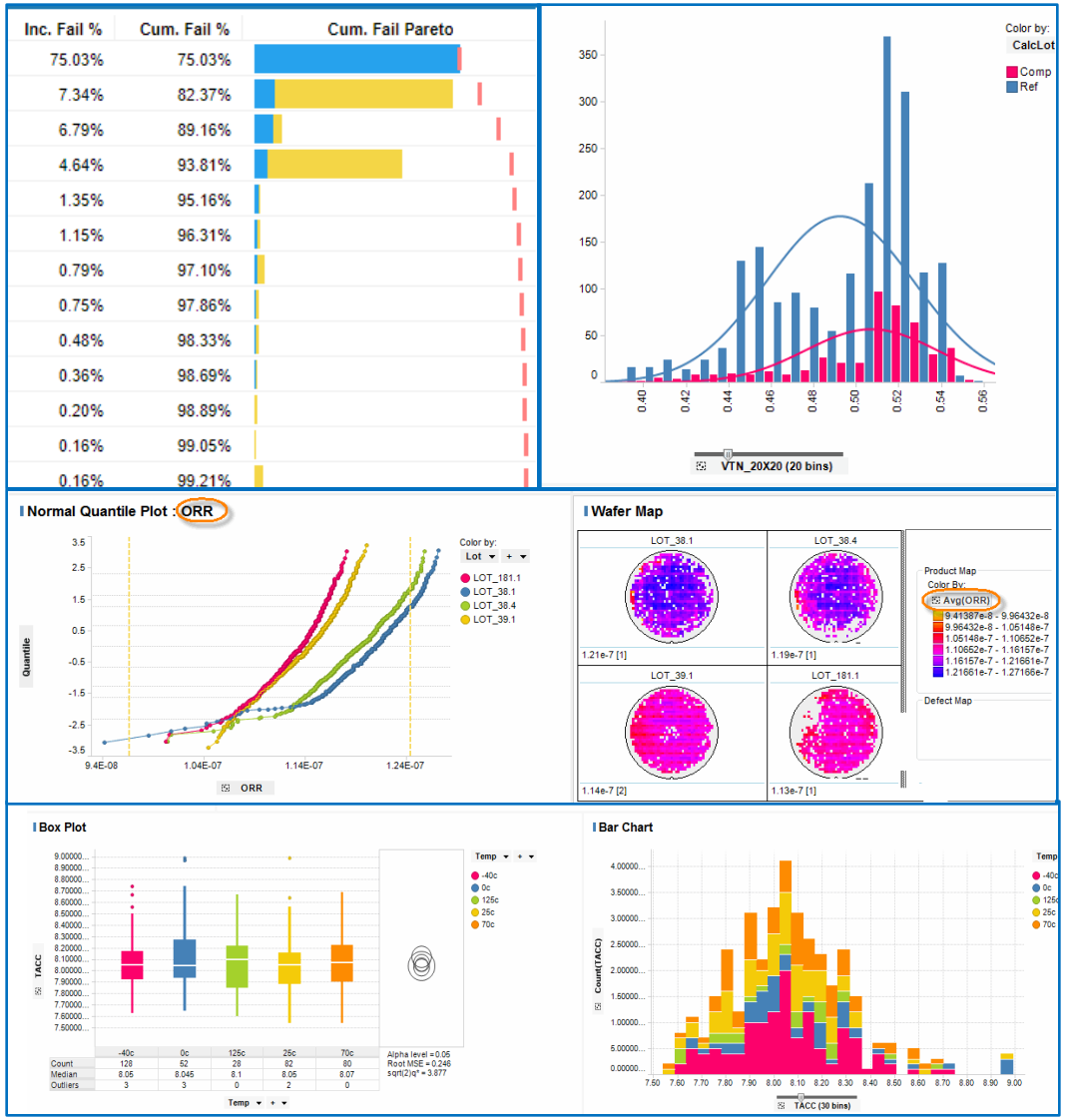
FASTER NPI Yield Ramp

NPI – New Product Introduction

New Product Introduction & Characterization Feature Matrix

Capability	Exensio Manufacturing Analytics	Partnership
Test Program Validation & Optimization		
Test Coverage (Never failing / Redundant tests)	✓	
Limits Analysis		
Specification, Guard band Limit Setting	✓	
Product Characterization		
Wide / Sweep Data Handling	✓	
CP / CPK Analysis, VDD / Temp Char Analysis	✓	
Fab / Supplier Matching & Qualification	✓	
Reporting / Templates / Release to Production	✓	
Design / Layout Sensitivities to Process		
WS / FT to WAT: Die Level Process Sensitivity	✓	
On Chip Agents	✓	✓
Fault Diagnostics		✓
Fab/Foundry		
Design layout sesnitivities	✓	
Split Lot Analysis	✓	



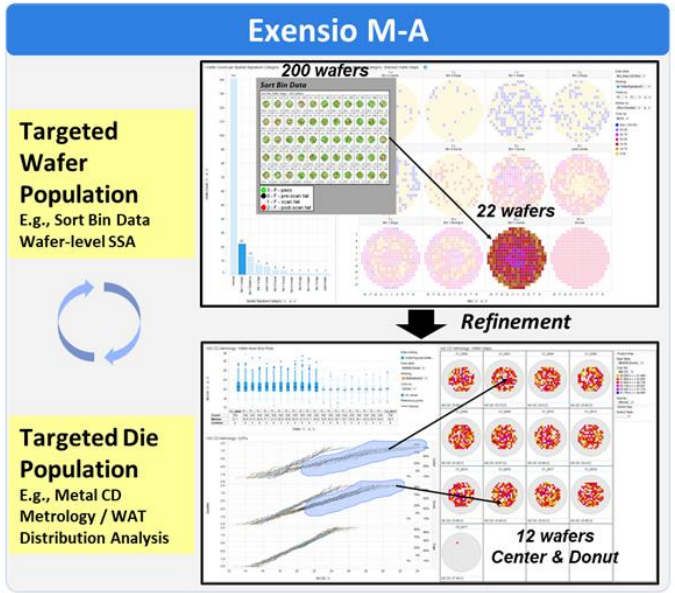
Yield Ramp

Yield Ramp & FA Diagnostics: Siemens Tessent + Exensio

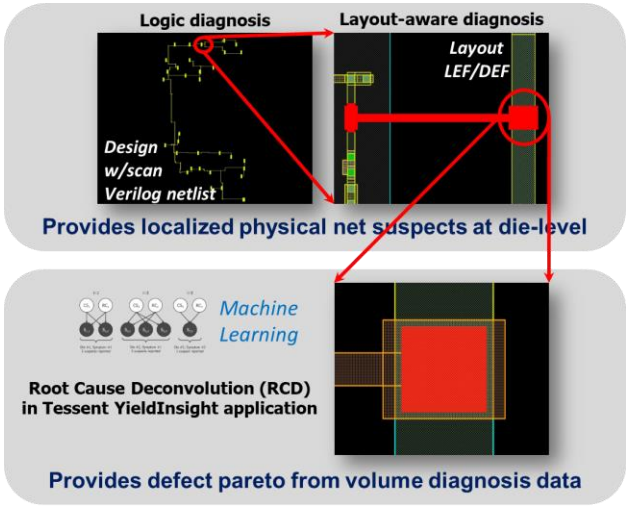
Locate & Identify Root Cause of Logic Failures

Locate and Identify Root Cause of Memory Failures

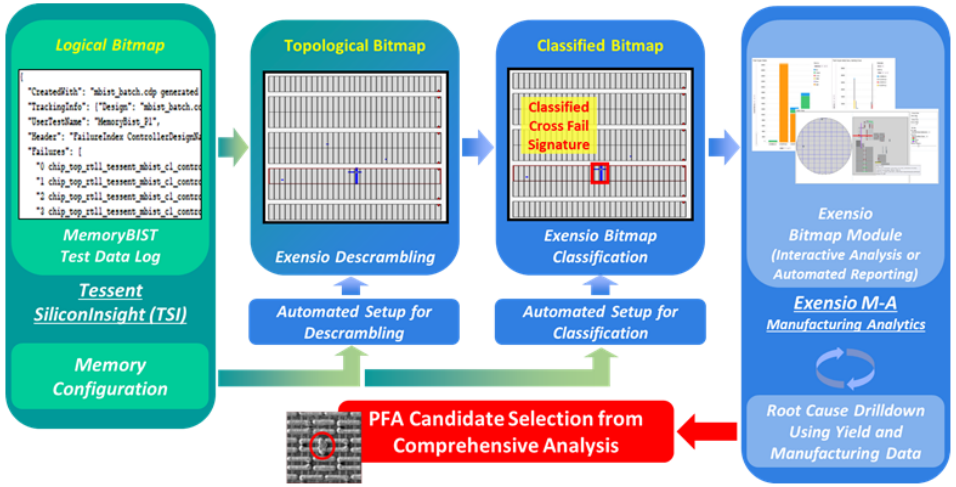
Exensio M-A: Home in on target population for biggest impact



Tessent YieldInsight: Localize defects for more effective logic PFA



Tessent SiliconInsight and Exensio M-A: Simplify and routinize effective memory bitmap



Partnership with Tessent for BIC debug and FA

HVM – High Volume Manufacturing

Exensio Advanced Quality & Ops Path

Operational Visibility

Operations Shield

Quality Shield

Machine Learning

BIC Ops

US and EU Best in Class suppliers are here

Are moving here

Quality Shield is essential for to compete with Best-in-Class

Exensio Advanced Quality & Ops Path

Offline Reporting
- *Floor Monitoring*
- *OEE reporting*
- *Stoppages / RE losses*

Real Time Rules
- *Outlier Screens (DPAT, GDBN)*
- *Escape Prevention (eg Test count)*

Operational Visibility | **Operations Shield** | **Quality Shield** | **Machine Learning**

Real Time Rules
- *Site2Site Yield*
- *UPH Limit*

Model Based Prediction
Model Based Screening
- *Predictive Binning*
- *ML Outlier Screening*
- *"Bring Your Own Model"*

BIC Ops

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Powerful Rules for OSATs and Fabless

Operations Shield

Process Control Rules

- Fab & Packaging Problems
- Test Floor Problems

Quality Shield

Escape Prevention Rules

- Stop errors from shipping
- Valid ECID

Quality Shield

Outlier Detection Rules

- Catch discrepant units

Powerful Rules for OSATs and Fabless: Detailed Rule Catalog

Process Control

- Yield
- Bin Percent / Count
- Lot Begin / End
- Parametric Test Statistic
- Parametric Test Yield
- Site-to-Site
  - Yield
  - Percent Delta
  - Test Statistic Delta
- Parametric Test SPC (WECO)
  - Oscillating / Outlier / Trend / Zone

Escape Prevention

- Consecutive Bin
- Stuck Unit (parametric)
- Test Count
- Bad Device Good Bin
- Good Device Bad Bin
- Limit Fail Good Bin
- Measurement Exception
- Limit Exception
- Device Test Time
- Retest Limit
- Mixed Lot Limit
- Units per Hour Limit
- Valid ECID

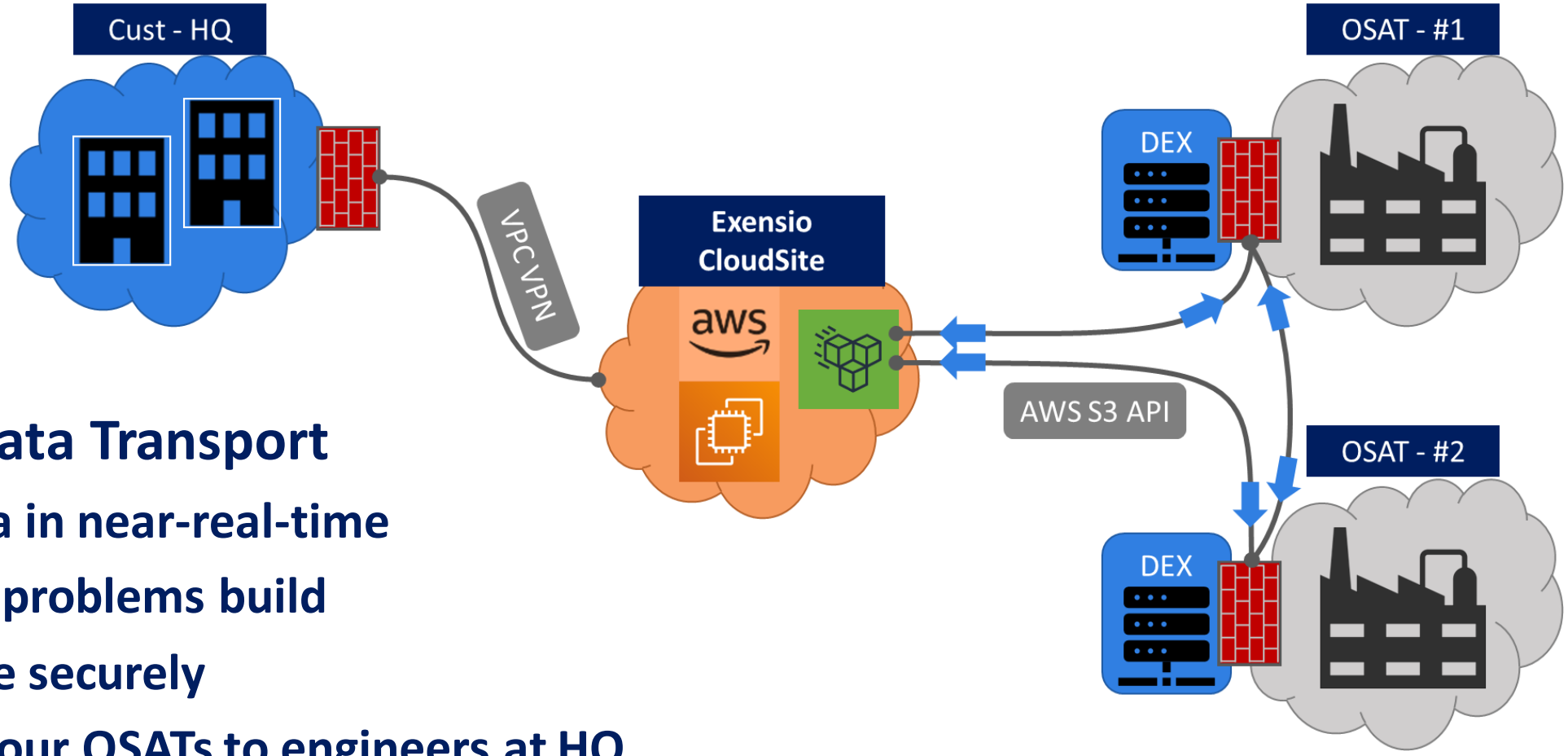
Outlier Detection

- DPAT
- GDBN
- Cluster Detection
- NNR
- Univariate / Multivariate
- Custom rules by equations

WECO Western Electric Co
SPC Statistical process Control
ECID Electronic/Exclusive Chip ID
DPAT Dynamic Part Average Test
GDBN Good Die Bad Neighborhood
NNR Nearest Neighbor Residual

Data Exchange (DEX) Connects You & Your Suppliers

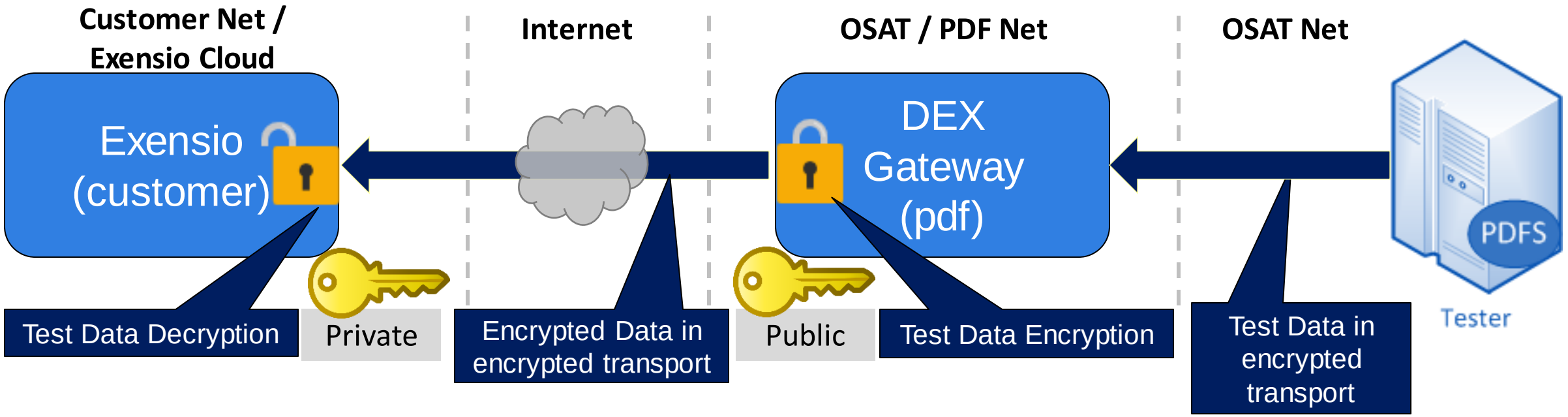
High-performance managed Exensio deployment with OSAT integration



Automated Data Transport

- Get your data in near-real-time
- React before problems build
- Communicate securely
- Connect *all* your OSATs to engineers at HQ

Security : Encrypted Data Transport (Example: OSAT to Customer)



- **Encrypted Transport Across Public Networks**
  - Transport between DEX and Exensio nodes is encrypted and private
  - Data is transmitted over encrypted tunnel
  - Only intended destination server can decrypt transport payloads
    - Node-unique private encryption key required to decrypt payloads
    - Bulk payload encrypted with AES-256

In-Field Failures

Automotive Doesn’t End with Device Shipment

Containment & Root Cause of Complex FAs

- **Despite all your teams' good efforts, you *will* get FAs (Failure Analysis Requests)**

- **Modern products getting more complicated**
  - Complex supply chains
  - Chiplets & 2.5D/3D packages
  - Advanced process nodes
- **But your customers don't care**
- **They want the answers, *now***

Traceability & End-to-End Data Analytics make FA easier

End to End Analytics & Traceability for Better FA/RMA

WAT (aka PCM, E-Test)

- Parametric data

Wafer Sort (aka EWS, CP)

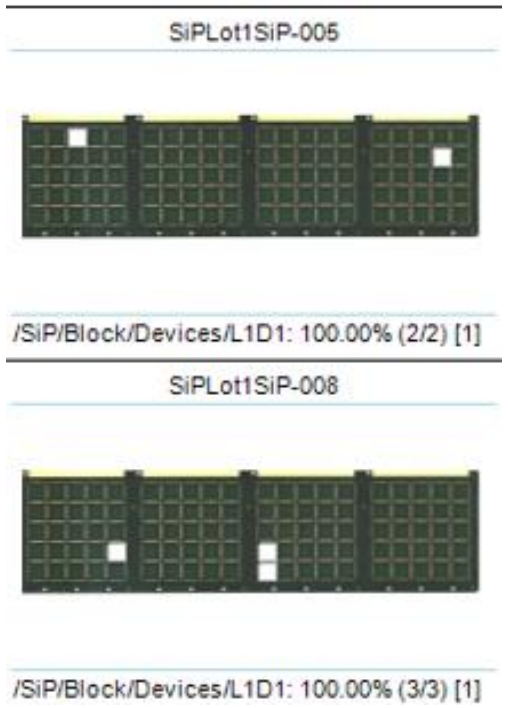
- Yield, binning
- Wafermaps
- Parametric data
- Equipment Details

Final Test (aka Class)

- Yield, binning
- Parametric Data
- Equipment Details

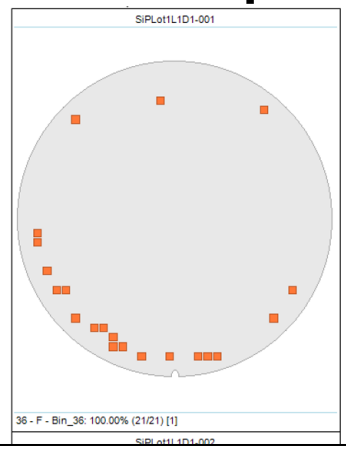
Packaging

- Substrate Maps



Reconstituted Wafer Maps

- ✓ Use traceability to see failures at each of previous steps
- ✓ ECID or Exensio Assembly Ops

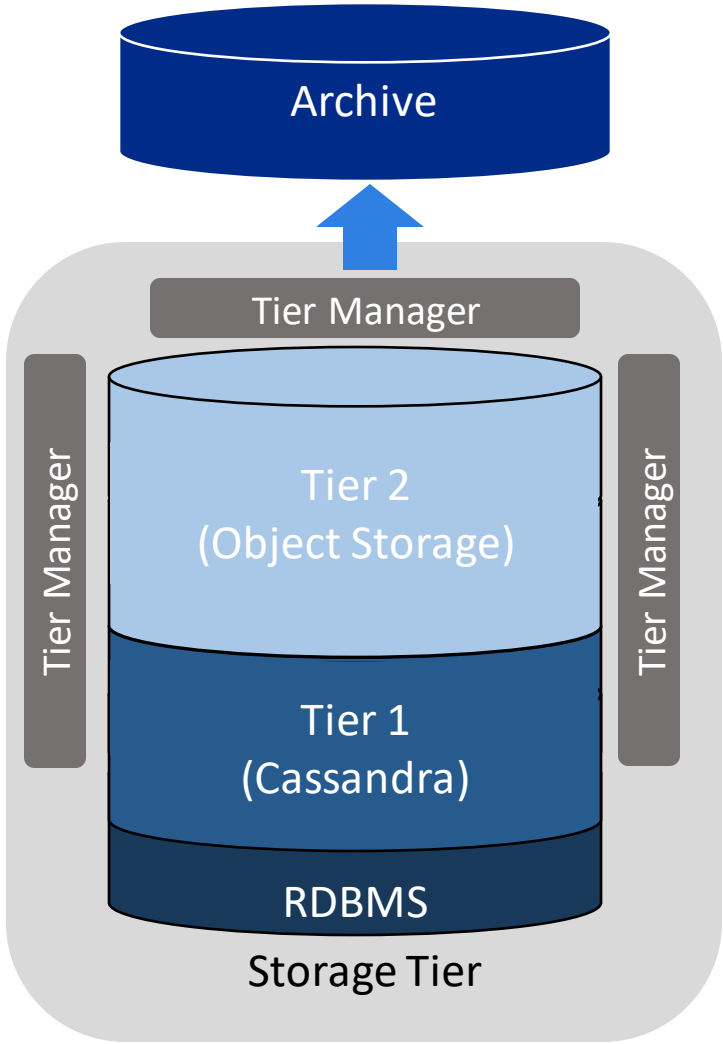


Defect Localization

- Logic using Scan Fault Diags
- Memory using Bitmap
- Both → Siemens Tessent collaboration

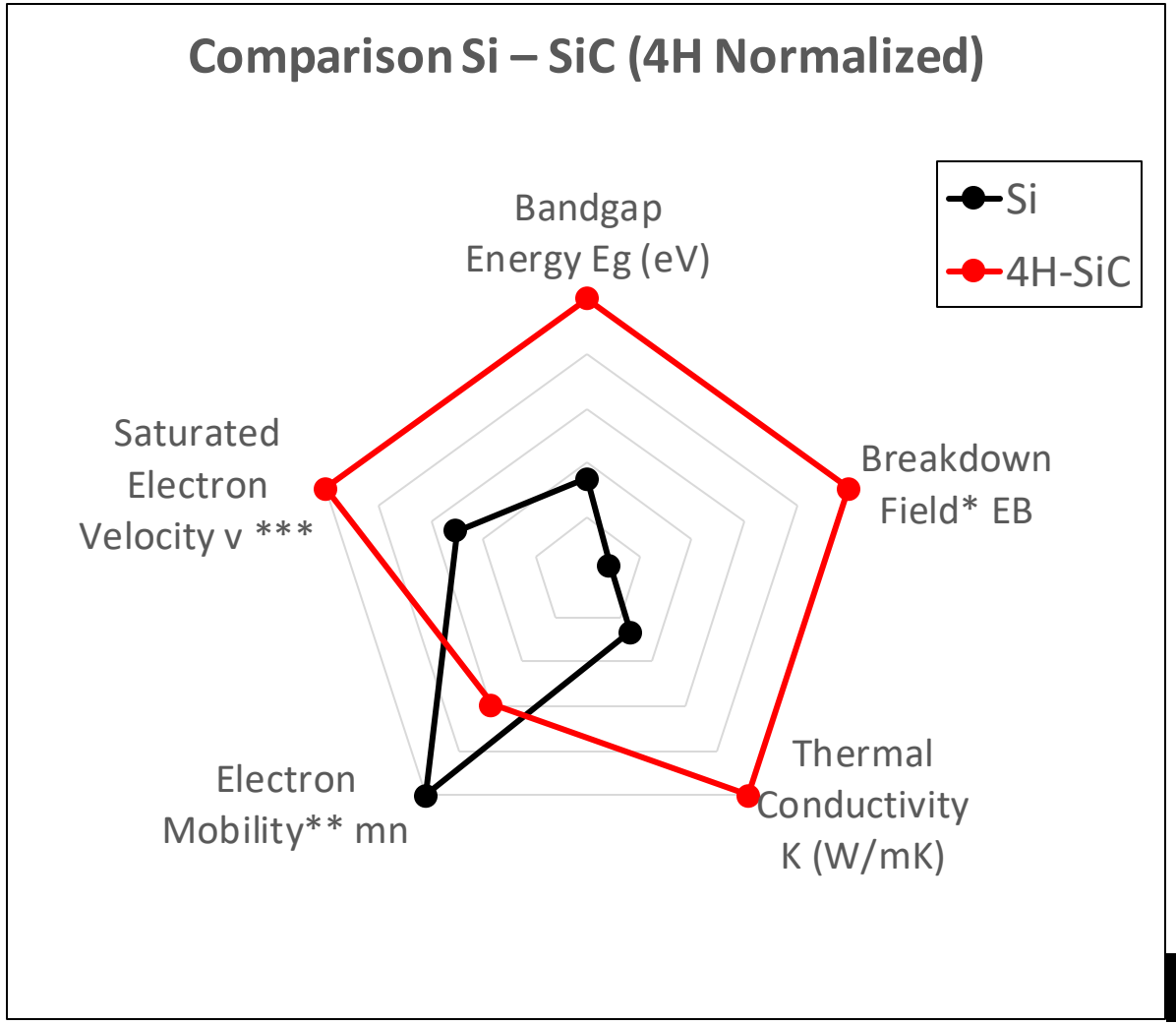
Exensio Cloud : Tiered Storage Benefits

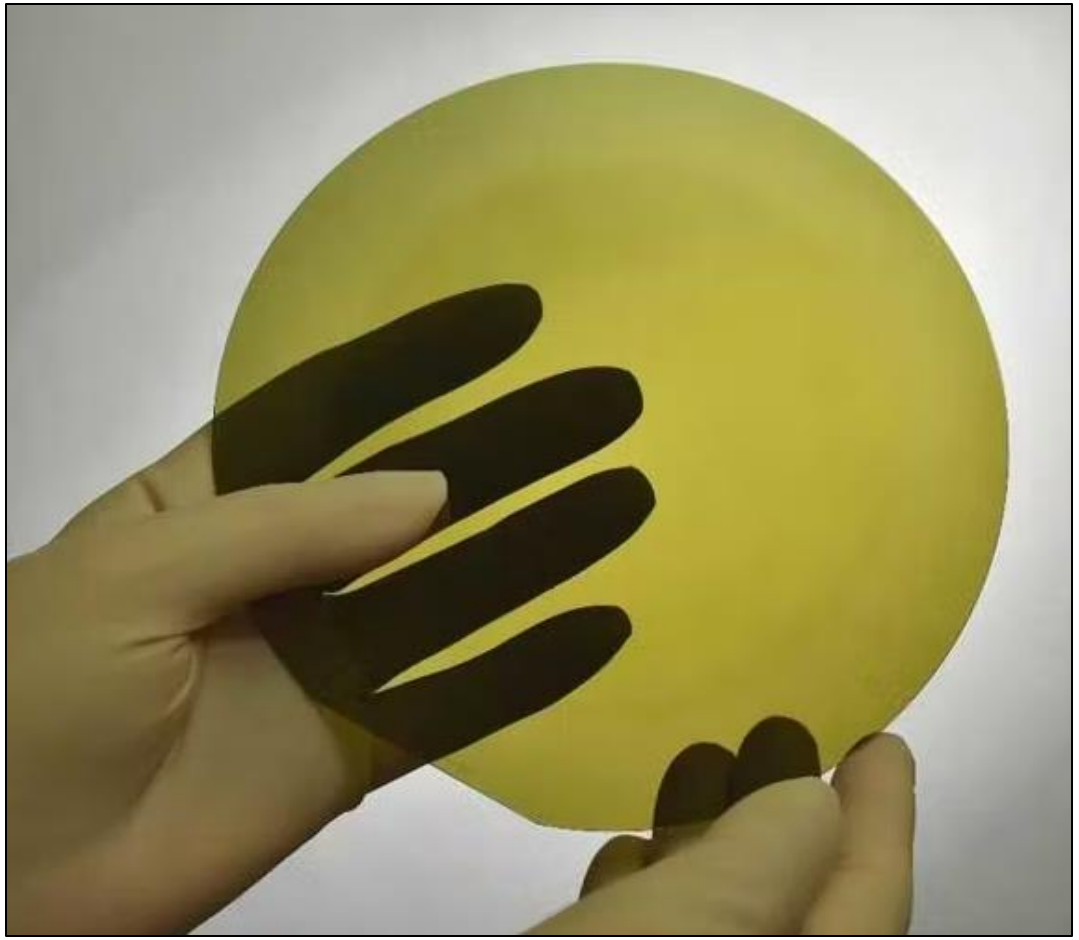
- **FA is impossible if you don’t keep the data**
- **Automotive – 10+ years data retention**
- **Keep your new data for fast retrieval**
- **Keep your old data for when you need it**
  - Rarely
  - But urgently
- **Seamless to users / Seamless to integration**



Solutions for SiC Devices

Silicon Carbide - Introduction





source: onsemi

Great for Power IC and RF

Challenges with SiC Manufacturing

- Complicated (in-house vs outsourced) material flow
- Lot reshuffling: wafer & lot genealogy
- High defectivity
- Equipment connectivity (150 & 200 mm)

→ covered in this talk

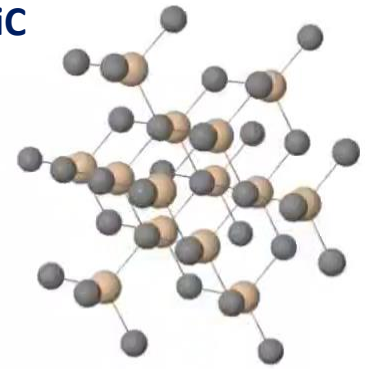
- Small pucks vs large boules
- New types of subsurface defects hard to detect with conventional means
- No wafer scribe or ambiguous wafer ID
- Defect sampling for SEM Review: too many
- Unpatterned vs patterned wafers: registration

→ inquire for more detail

Compound Semiconductor: stoichiometry matters!

>250 polytypes: stacking faults are common

SiC



source: ChemTube3D

SiC Package for Fabs and IDM's

Fault Detection & Classification (FDC)

Traceability & E142

Genealogy for Substrates and Wafers

ModelOps with AI/ML

- Improve crystal (boule) growth
- Manage equipment fleet
- Identify root-cause of defects

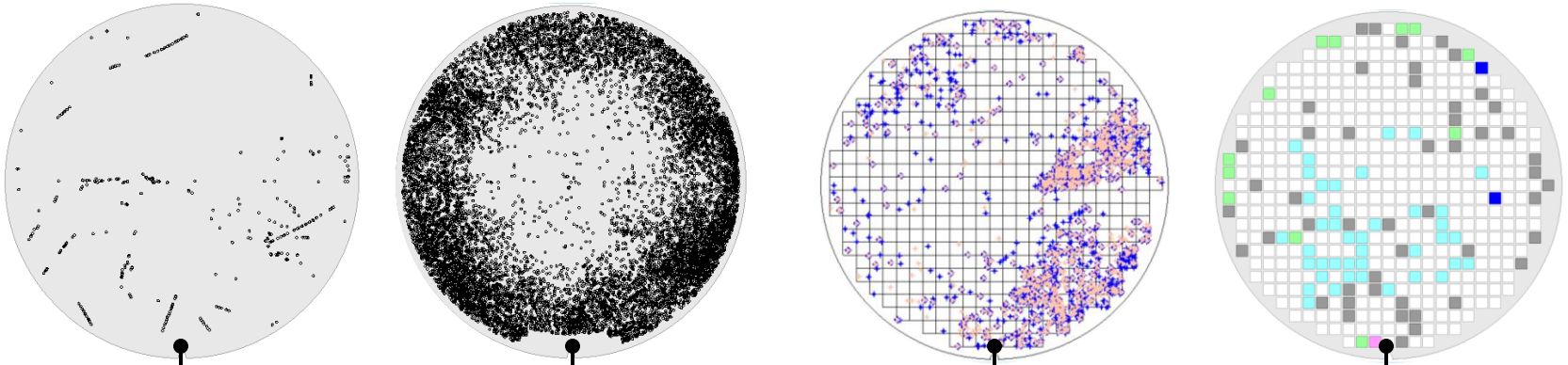
- Predictive burn-in
- Shift-left strategy to increase yield
- Streamline RMA's

'boule' & Substrate → Epi → Wafer Processing → Wafer Test → Packaging Assembly → Burn-in & Final Test

SiC Defectivity

"SiC is where silicon was decades ago…"

$$$



'boule' & Substrate → Epi → Wafer Processing → Wafer Test → Packaging Assembly → Burn-in & Final Test

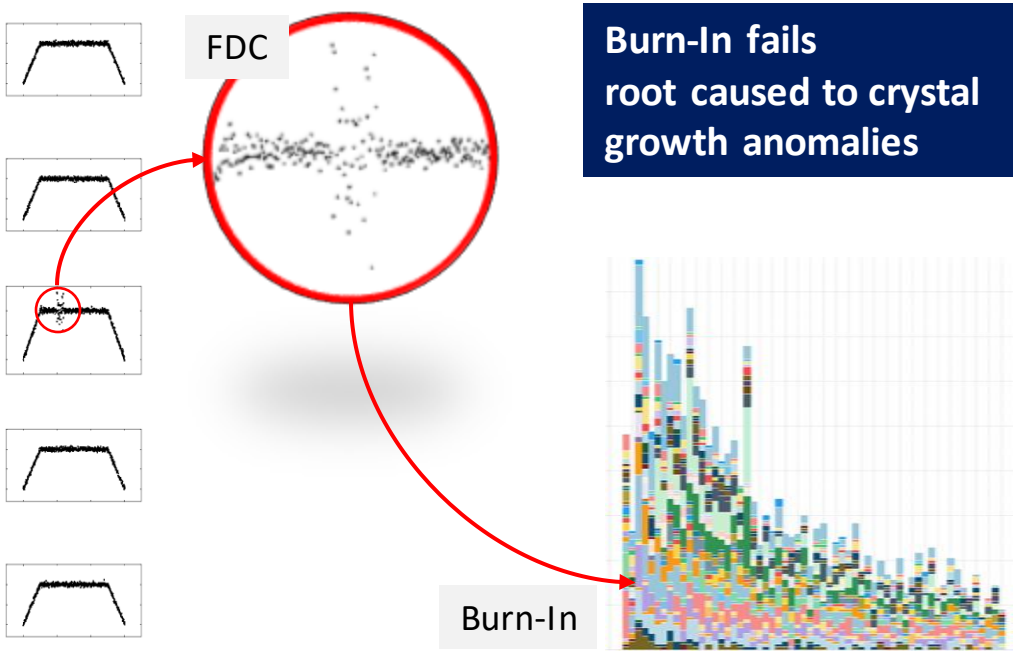
Pdf representative data

Deployment Examples in SiC Manufacturing

IDM "C":
True End-to-End Deployment

IDM "B":
Fab, Sort & Assembly

IDM "A":
Exensio Manufacturing Analytics – Fab only

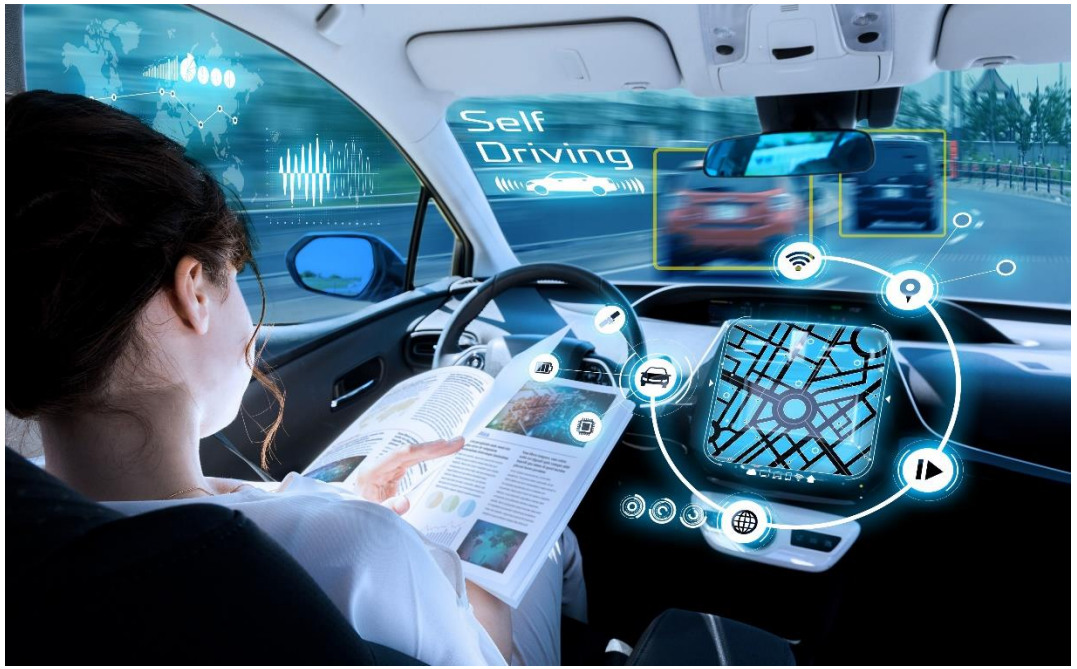


Burn-In fails root caused to crystal growth anomalies

'boule' & Substrate → Epi → Wafer Processing → Wafer Test → Packaging Assembly → Burn-in & Final Test

Conclusion

- **Electrification & ADAS driving rapid growth**
- **Many new entrants**
- **PDF: broadest and deepest analytics solution**
- **With specialized offerings**
  - SiC package for EV products



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