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2023 PDF Users Conference:

AI for tomorrow's manufacturing and R&D

Location:

Santa Clara Marriott - 2700 Mission College Boulevard Santa Clara, California 95054 USA

Solutions for Fabless

Presented by Marc Jacobs October 23, 2023 This presentation and discussions resulting from it may include future product features or fixes, or the expected timing of future releases. This information is intended only to highlight areas of possible future development and current prioritizations. Nothing in this presentation or the discussions stemming from it are a commitment to any future release, new product features or fixes, or the timing of any releases. Actual future releases may or may not include these product features or fixes, and changes to any roadmap or timeline are at the sole discretion of PDF Solutions, Inc. and may be made without any requirement for updating. For information on current prioritizations and intended future features or fixes, contact sales@pdf.com.

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End-to-end Integrated Platform for Semiconductor Analytics



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Fabless Product Lifecycle

Design	• Sensors
NPI/Char	 Managing Wide Data Characterization
Yield Ramp	 Accelerating Yield Analysis Machine Learning for Optimized Test Adaptive Test System Scalability
HVM	 Best-in-Class Operations at Test Supply Chain Visibility & Security Leveling Up Your Engineers Executive View
In-Field	Failure Analysis & Returns

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Design Phase Challenges & Solutions



Sensors for Performance, Reliability & System in Package (SiP)

In-die Sensors for Performance, Reliability and SiP



CV® Core: A view into the health of die fundamentals



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NPI Challenges & Solutions



- Managing Wide Data
- Characterization

Managing Wide Data – The "Test Item Explosion"

- IP instances multiplying AND char complexity multiplying
- Modern complex SOCs have millions of test items
 - Especially during characterization and NPI
- RF or Analog example: Frequency Sweep tests on ATE
 - Repeat test across range of input frequencies
 - Limits may vary, too
- Digital example: Shmoo test on ATE
 - Conventional shmoo example: 2D V_{dd} vs f_{clock}
 - Challenging shmoo: 3D V_{dd} vs f_{clock} vs Register Setting
- NPI Engineer wants
 - Load all my data at once
 - Analysis must be speedy

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Managing Wide Data – The "Test Item Explosion"

Recent versions of Exensio have implemented improvements

- Leveraged big data Spark & Cassandra cluster architecture
- Plus novel data integration techniques

Initial benefits shown below

Data Type	Retrieval Type	Number of Columns	Demonstrated Improvement
>1 M Parametric	Summary on the Fly	>1 M columns	Up to 11x
Results	Raw Data Retrieval	>1 M columns	Up to 55x
Parametric Pass/Fail	Continue-on-Fail Analysis	>1 M columns	Up to 35x

New Product Introduction & Characterization Feature Matrix

Capability	Exensio	Partnership	Inc. Fail %	Cum. Fail %	Cum. Fail Pareto	Color by: 350 - CalcLot
	Manufacturing		75.03%	75.03%		Comp Ref
	Analytics		6.79%	89.16%	· ·	300 -
Test Program Validation & Optimization			4.64%	93.81%	1	250
Test Coverage (Never failing / Redundant tests)	\checkmark		1.35%	96.31%		150 -
Limits Analysis			0.79%	97.10% 97.86%		
Specification, Guard band Limit Setting			0.48%	98.33%	1	50
Product Characterization			0.36%	98.89%		0.40 0.42 0.46 0.46 0.50 0.52 0.52 0.54 0.55 0.55
			0.16%	99.05%	Í	
Wide / Sweep Data Handling	\checkmark		0.16%	99.21%		S VIN_20420 (20 bins)
CP / CPK Analysis, VDD / Temp Char Analysis	\checkmark		3.5		Color by:	LOT_38.1 LOT_38.4
Fab / Supplier Matching & Qualification	\checkmark		2.5		LOT_181.1 LOT_38.4 LOT_39.1	Product Map Cover By Cover By
Reporting / Templates / Release to Production	\checkmark		-0.5 -			12167[1] 1196-7[1] 1196-7[1] 105225-7-110512-7 105225-7-110512-7 105225-7-110512-7 105225-7-110512-7 105225-7-110512-7 105225-7-110512-7 121661-7-127108-7
Design / Layout Sensitivities to Process			-1.5			Defect Map
WS / FT to WAT: Die Level Process Sensitivity	\checkmark		-3.5 9.4E-0	8 1.04E-07	1.14E-07 1.24E-07	1.14e-7[2]
On Chip Agents	\checkmark		Box Plot		• Temp ▼ + ▼	I Bar Chart
Fault Diagnostics		\checkmark	8.80000 8.70000 8.60000 8.50000 8.40000		● - 40c ● 0c ● 125c ● 255 ● 70c	3 5000
Fab/Foundry			8.30000 8.20000 8.10000 7.90000 58 7.80000	\$ \$ \$		
Design layout sesnitivities	V .		7.70000 7.60000 7.60000	-400 00 1250	25c 70c Alaba Juni - 0.05	
Split Lot Analysis	\checkmark		Count Median Outliers	128 52 28 8.05 8.045 8.1 3 3 0 Temp	62 00 Projeta Projeta Vode 805 8.05 8.07 Sant'2)q* = 3.877 2 0	0.00000 7.50 7.50 7.70 7.50 7.50 8.00 8.10 8.20 8.30 8.40 8.50 8.50 8.50 8.50 8.50 37 TACC (30 bins)

Flexibility to link customized templates in Guided Analytics (GA)

Use the power and simplicity of Guided Analytics to speed your Characterization analysis



Characterization Features for the Way You Work

- Bin pareto view where are the losses?
- Parametric view are limits appropriate for results?
- Toggle switching between the two views

Bin Pareto



Parametric



Yield Ramp Challenges & Solutions



- Accelerating Yield Analysis
- Machine Learning for Optimized Test
- Adaptive Test

PDF Solutions and Siemens EDA accelerating yield



How to get to high yield faster?

- Integrate diagnostics to FIRE/DirectScan
- Combine Fault Diagnostics with all your data sources
 - -WAT
 - Sort Yield
 - Sort Maps
 - Etc.

Get to root cause faster

- Find layout dependency
- Help the foundry to know where to look for PFA

Tessent and Exensio/FIRE working together



Customer Benefit

For an HVM product at advanced node:

- 7x improvement in inspection and/or PFA efficiency
- ID'd root causes for ~90% of measured failure

The system in package (SiP) testing challenge



For SiP

- P/F is not enough
- Rules are not enough
 → Move to models
- Pass info to downstream tests

Feed Forward, Model-Based Testing



Deploy a feed-forward-loop test operation for a multi-chip device

- Reliable and timely capture of wafer sort test operation data
- Automate feature extraction from PCM/WAT & WS to produce feed-forward data
- Mechanism to train & periodically retrain models on current data
- Deploy models across supply chain to the package test operation
- Monitor test data and model performance

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Edge Integrated Inference Container

Your model with Exensio rules & model management deployed to the edge



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Adaptive Test Architecture

Test flow switching controlled by Customer recipe

- Short flow when conditions nominal
- Increase test coverage when conditions abnormal
- Sample monitor all tests for quality and analytic

DTC Dynamic Test Controller

test control / data reporting / rule engine

Agent Tester Agent

tester specific / data capture / TOS interface

Client Test Program Client

flow switching / dynamic limits / Exensio APIs



Cloud for Scalability

Use Exensio in the Cloud to manage your scaling

- Focus on your ramp
- Not your data management
- Automated Node Expansion for data scalability
- High Availability and Disaster Recovery



HVM Challenges & Solutions



- Best in Class Operations at Test
- Supply Chain Visibility & Security
- Leveling Up Your Engineers

Exensio Advanced Quality & Ops Path



GDBN Good Die Bad Neighborhood

BiC Best in Class



Drive Operational Efficiency Improvement

Real-Time Test Status

Throughput (UPH) Analysis

Actual UPH vs target UPH by Product / Tester / Test Program

Overall Equipment Efficiency (OEE) Analysis

- Efficiency by Floor / Shift / Tester
- Measure Setup and Intra-Lot Idle Time



Efficiency by Floor

Floor Name

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Fail Bin Distribution

Selected Fail Bin By Site

3 2

OF

Last N Touchdowns : 25 Bin Type : Soft Bin V

Last 25 Touchdowns

Data limited b

Data table: DieData

Markino

Marking

Marker by: (Row Num

Color by: PASS + +

V 82% ~~~ 84% VIMV

76% VM

140

138

136

134

132

130

128

M.M. 64% VM.M. 99%

Powerful Rules for OSATs and Fabless

Operations Shield

Process Control Rules

- Fab & Packaging Problems
- Test Floor Problems

Quality Shield

Escape Prevention Rules

Stop errors from shipping

Quality Shield

Outlier Detection Rules

Catch discrepant units

Powerful Rules for OSATs and Fabless: Detailed Rule Catalog

Process Control

- Yield
- Bin Percent / Count
- Lot Begin / End
- Parametric Test Statistic
- Parametric Test Yield
- Site-to-Site
 - Yield
 - Percent Delta
 - Test Statistic Delta
- Parametric Test SPC (WECO)
 - Oscillating / Outlier / Trend / Zone

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Escape Prevention

- Consecutive Bin
- Stuck Unit (parametric)
- Test Count
- Bad Device Good Bin
- Good Device Bad Bin
- Limit Fail Good Bin
- Measurement Exception
- Limit Exception
- Device Test Time
- Retest Limit
- Mixed Lot Limit
- Units per Hour Limit
- Valid ECID

Outlier Detection

- DPAT
- GDBN
- Cluster Detection
- NNR
- Univariate / Multivariate
- Custom rules by equations

WECO Western Electric Co SPC Statistical process Control ECID Electronic/Exclusive Chip ID DPAT Dynamic Part Average Test GDBN Good Die Bad Neighborhood NNR Nearest Neighbor Residual

Data Exchange Connects You & Your Suppliers

High-performance managed Exensio deployment with OSAT integration



Exensio Data Exchange via DEX



Exensio DEX

- Local test data collection and tester integration
- Bidirectional secure data transport
- Customer data routing
- End-to-end encryption
- Secure containerized model execution

Security : Encrypted Data Transport (Example: OSAT to Customer)



Encrypted Transport Across Public Networks

- Transport between DEX and Exensio nodes is encrypted and private
- Data is transmitted over encrypted tunnel
- Only intended destination server can decrypt transport payloads
 - Node-unique private encryption key required to decrypt payloads
 - Bulk payload encrypted with AES-256

Oct 2023 DEX Deployment Locations (OSATs)

DEX ID	Site Name	
AMKOR-P3/4	Amkor Philippines	
AMKOR-TW	Amkor Taiwan	
ASE-CL	ASE Chungli	
ASE-KH	ASE Kaohsiung	
Carsem-S	Carsem Malaysia S-Site	
FOX-TW	Foxconn Taiwan/Ingrasys	
GIGA-TW	Giga Taiwan	
ITEST	iTest Milpitas	
JCET-SG	JCET Singapore/STATS ChipPAC	
JSET-CN	JCET China	

DEX ID	Site Name
KYEC-ZN	KYEC ZhuNan
SPIL-CS	SPIL Chung Shan
SPIL-HC	SPIL Hsinchu
SPIL-SZ	SPIL SuZhou
SPIL-ZK	SPIL Zhong Ke
UTAC-SG	UTAC Singapore
UTAC-TH	UTAC Thailand
KYEC-LFT	KYEC Tunlou
GIGA-TW	ChipBond Taiwan
UNISEM	Unisem Malaysia







Exensio User and/or DEX

DEX

New in Q3/Q4 '23



10 new sites added / in-process since Q2 '23

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Guided Analytics: Continuous Data Mining on 100% of data

Manual analysis typically evaluates monthly 3-5% of the data

- Significant time spent aligning data types
- Focus on obvious excursions and low yields
- Harder to analyze wafer patterns, correlations across data types



Guided Analytics systematically analyzes 100% of the aligned data* and highlights issues

- Single database with aligned data allows for consistent results and more sophisticated analysis
- Structured GA flow provides consistency in analysis across the organization

Processes all data every day

*Data types: Yield, Hard/Soft Bins, failing test parameters, PCM/WAT, test equipment, UPH

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Guided Analytics for Fabless Companies

Automates up to 90% of analysis; Quickly review with few clicks

- High level dashboard
- At-a-glance prioritization across products
- Ultra-fast performance
- Analyze all your data types
 - Seamless integration of data types: Hard Bin, Soft Bin, parametric, WAT/PCM, test tools, UPH, etc.

Easy to customize analysis

- Tailor for how your company works
- Jump off for detailed analysis



Not only does GA make it easy to use the software, it makes it easy for engineers to do their jobs

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Guided Analytics for Execs: Look Across Your Business

- Higher level summarization
 - View by factory, product line, etc
- Overall view
 - Yield
 - Efficiency
 - Quality
- Know where to look
- Know where to delegate

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Executive View

Exec View: Loss Calculator

- Calculator function to translate losses into dollars.
- Both unit losses & wasted tester hours



In Field Challenges & Solutions



Containment & Root Cause of Complex FAs

Containment & Root Cause of Complex FAs

Despite all your teams' good efforts, you will get FAs

Modern products are complex

- Chiplets & 2.5D/3D packages
- Advanced process nodes
- Complex supply chains
- But your customers don't care
- They want the answers, now

Traceability & End-to-End Data Analytics make FA easier

End to End Analytics & Traceability for Better FA/RMA

■ WAT (aka PCM, E-Test)

– Parametric data

■ Wafer Sort (aka EWS, CP)

- Yield, binning
- Wafermaps
- Parametric data
- Equipment Details

Final Test (aka Class)

- Yield, binning
- Parametric Data
- Equipment Details

Packaging

– Substrate Maps

SiPLot1SiP-005



/SiP/Block/Devices/L1D1: 100.00% (2/2) [1]

SiPLot1SiP-008



/SiP/Block/Devices/L1D1: 100.00% (3/3) [1]

Reconstituted Wafer Maps

- ✓ Use traceability to see failures at each of previous steps
- ✓ ECID or Exensio
 Assembly Ops



Defect Localization

- Logic using Scan Fault Diags
- Memory using Bitmap
- Both → Siemens Tessent collaboration

Exensio Assembly Operations Overview

- Reduce yield loss by up to 10%
- Up to 5x faster RMA response & root cause analysis
- Up to 10x reduction in recall volume

WLP / PLP

TnR

Integrated with Exensio[®] Manufacturing Analytics



- Traceability through assembly and final test
- With or without ECIDs
- Enables NPI, yield ramp, device matching, RMA, ...
- Equipment integration via SECS GEM and Cimetrix[®] Sapience
- Full SEMI E142 support



Packaging



Final Test

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Chiplets

HBM, ...

Summary: PDF is solving real challenges with analytics-driven outlook



PDF's Mission: Provide innovative solutions to create, access, and organize data to enable analysis and control for semiconductor and electronics companies to achieve better time-to-market, yields, quality, and operational efficiencies

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Thank You

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