PDF/SOLUTIONS™

Confidential Information

SIEMENS

Improve yield by addressing layout pattern systematic defects

Jayant D’Souza (Siemens)

October 2023

Agenda

- Industry trend and problem statements
- Overview of solution
- Silicon results
- Key takeaways

Acknowledgement

PDFSolutions:

- Thomas Zanon
- Christian Sendner
- Hans Eisenmann

Siemens:

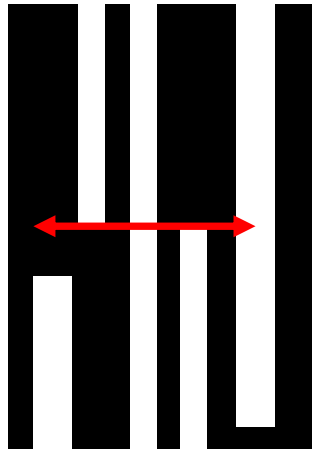
- Gaurav Veda
- Randy Klingenberg
- Manish Sharma

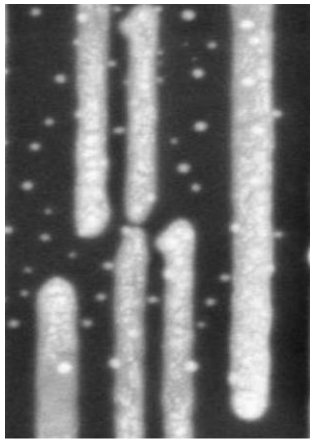
Industry trend

- Yield can be impacted by a variety of different factors at all technology nodes
  - Random
  - Systematic
  - Parametric
- Most systematic issues that are the combination of process, design and layout are ironed out early in early ramp and during NPI
- However, in advanced technology nodes, systematic yield issues remain a dominant concern throughout the product lifecycle
  - Could impact yield 2-4% points even in HVM

Problem definition: Identifying layout systematics

- Certain layout patterns can lead to systematic yield loss
  - new node, NPI, excursions in volume production
- Such patterns are highly actionable for improving yield
  - Leads to root cause identification
  - Foundry: process change
  - Fabless: design change
- How do we identify these patterns from volume scan diagnosis data?





C. Schuermyer, et.al. (MGC, GF), “Identifying Systematic Critical Features Using Silicon Diagnosis Data”, ASMC 2012

Patent pending

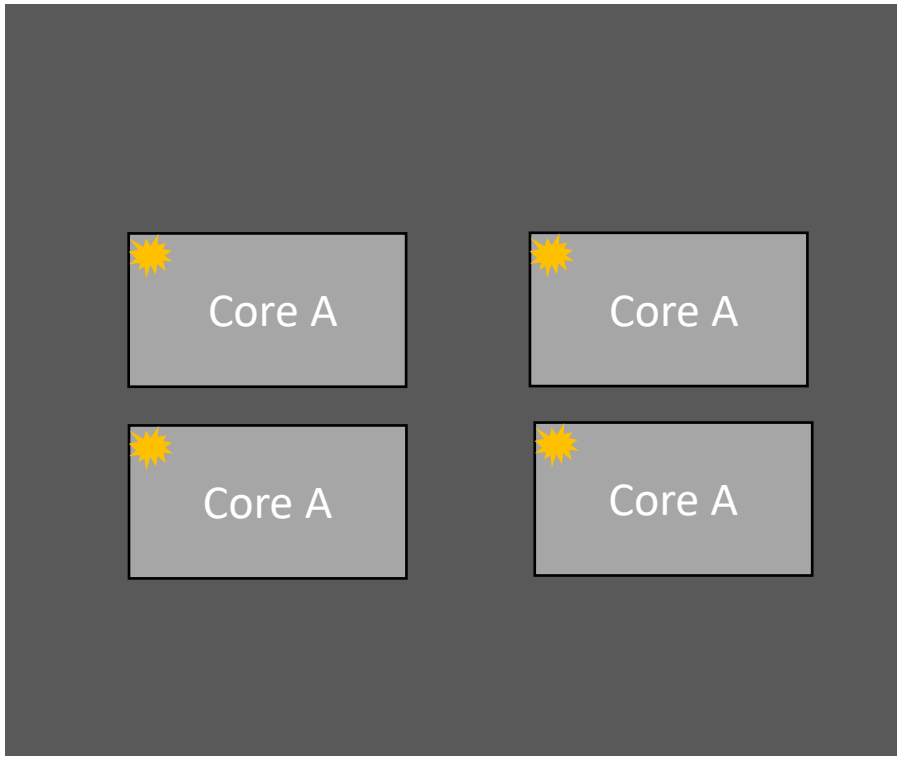
Repeater sets in Tessent diagnosis data

- A repeater set is a set of identical diagnosis reports (all suspects are the same)

- **These are most likely caused by a layout pattern**

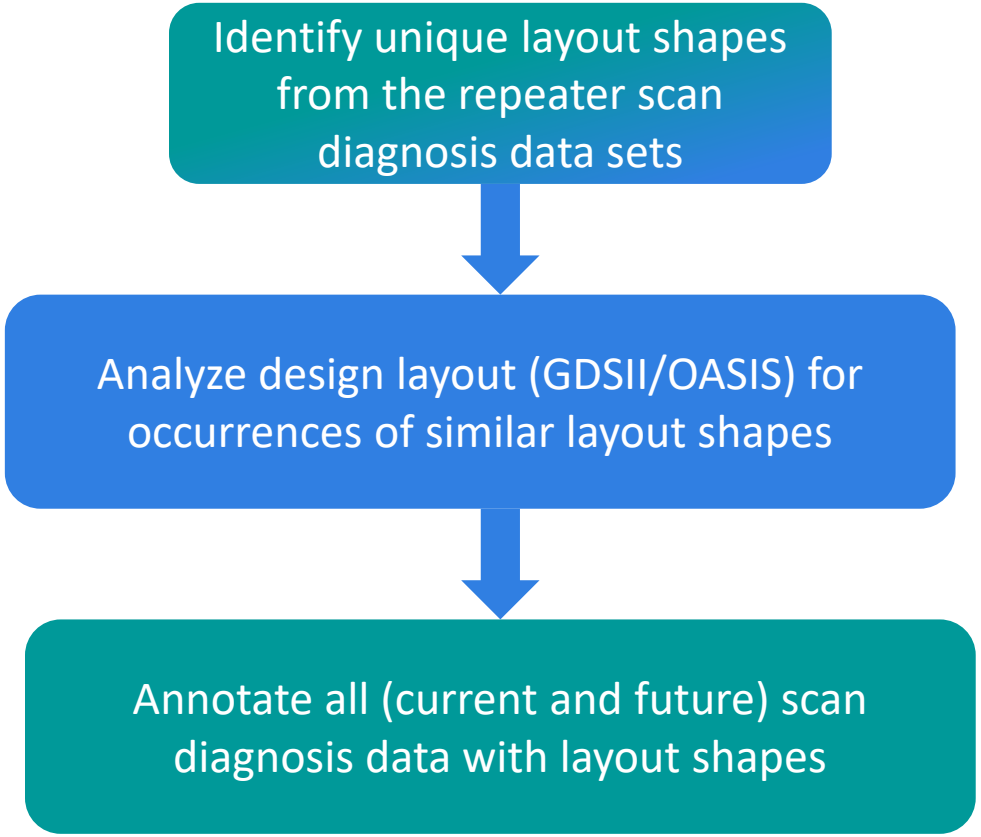
```
#symptoms=1 #suspects=16 CPU_time=9.79sec fail_log=OpenPattern_1_wafer1_41_66.flog.gz
#failing_patterns=92, #passing_patterns=128
#unexplained_failing_patterns=0


symptom=1 #suspects=16 #explained_patterns=92
43    52    63    64    90    91    101   125   127   153
171   195   204   231   238   240   313   315   322   323
336   337   345   353   363   368   371   372   378   395
411   423   454   466   497   499   525   540   541   547
559   561   578   597   607   609   635   662   663   666
668   672   694   697   707   711   712   718   725   733
744   746   748   764   789   810   813   826   833   855
856   863   867   877   887   897   905   908   918   926
936   937   941   945   952   955   957   960   962   964
965   968
suspect  score fail_match pass_mismatch type          value  pin_pathname cell_name net_pathname layout_status
-------------------------------------------------------------------------------------------------
1        100   92         0              STUCK         0      /p17/pic2/idec/i_0_105/A2 OR2_X1 /p17/pic2/drc_ipo_n67  INPUT_PIN_FAULT
     #potential_open_segments=3, #total_segments=43,   #potential_bridge_aggressors=0, #total_neighbors=na
     suspect  score fail_match pass_mismatch type          value  location layout_layer critical_area
     ---------------------------------------------------------------------------------------------
     1.1      100   92         0              OPEN          0      B13 metal1          1.29E-02
                                                                    via1            3.08E-03
                                                                    metal2          2.58E-02
                                                                    via2            3.08E-03
                                                                    metal3          1.29E-02
     1.2      100   92         0              OPEN          0      B11&B13&B21&B22 metal3          1.29E-02
                                                                    via3            3.08E-03
                                                                    metal4          9.62E-03
     1.3      100   92         0              OPEN          0      B11&B13&B22 metal3          9.38E-02
     ---------------------------------------------------------------------------------------------
```



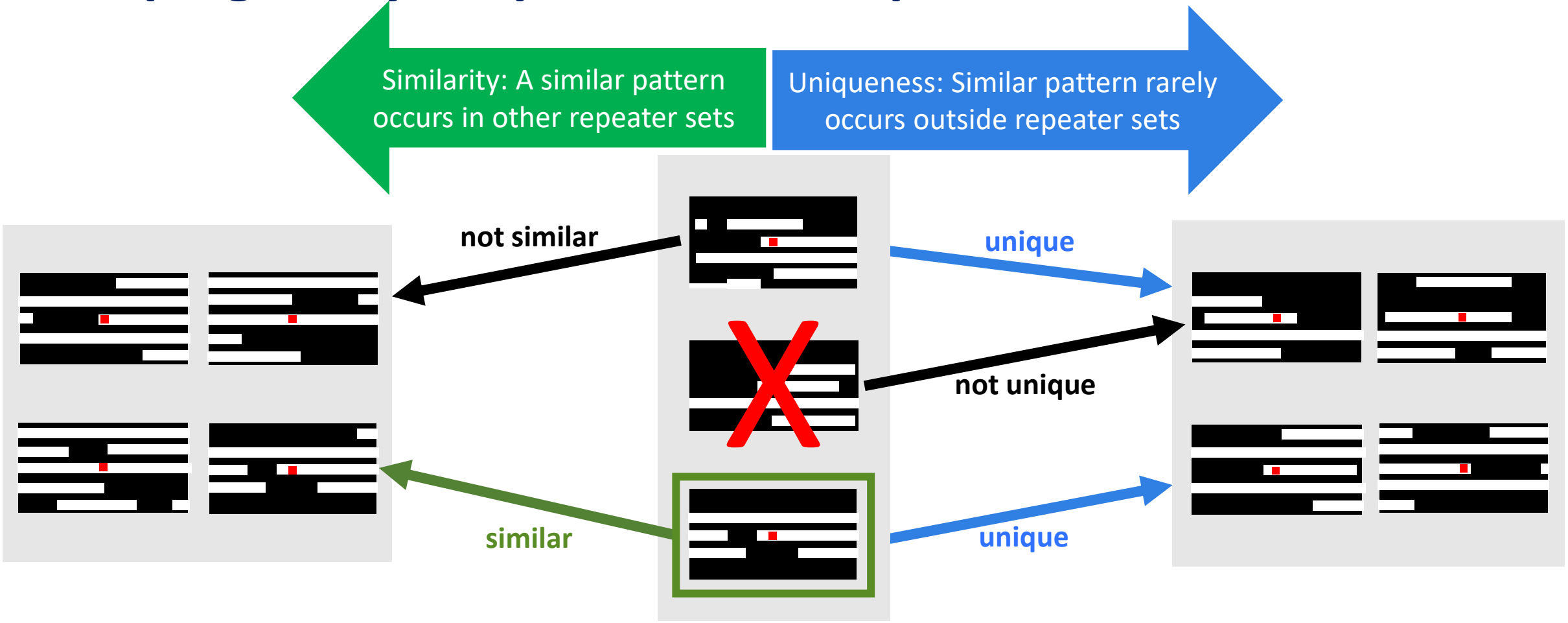
Approach

Patent pending



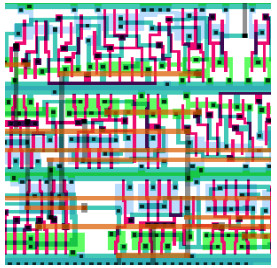
Patent pending

Grouping of layout patterns – unique and similar

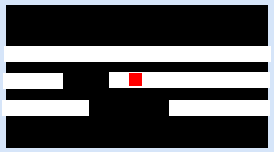


Full-chip extraction of layout pattern systematics using FIRE

Full-chip product design layout



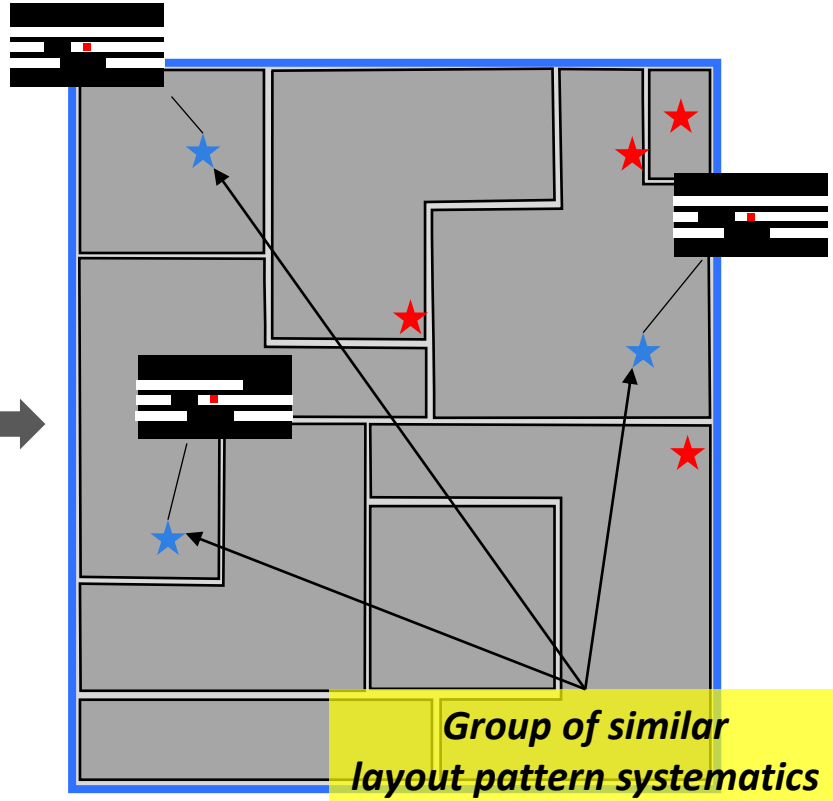
Layout pattern systematic candidates



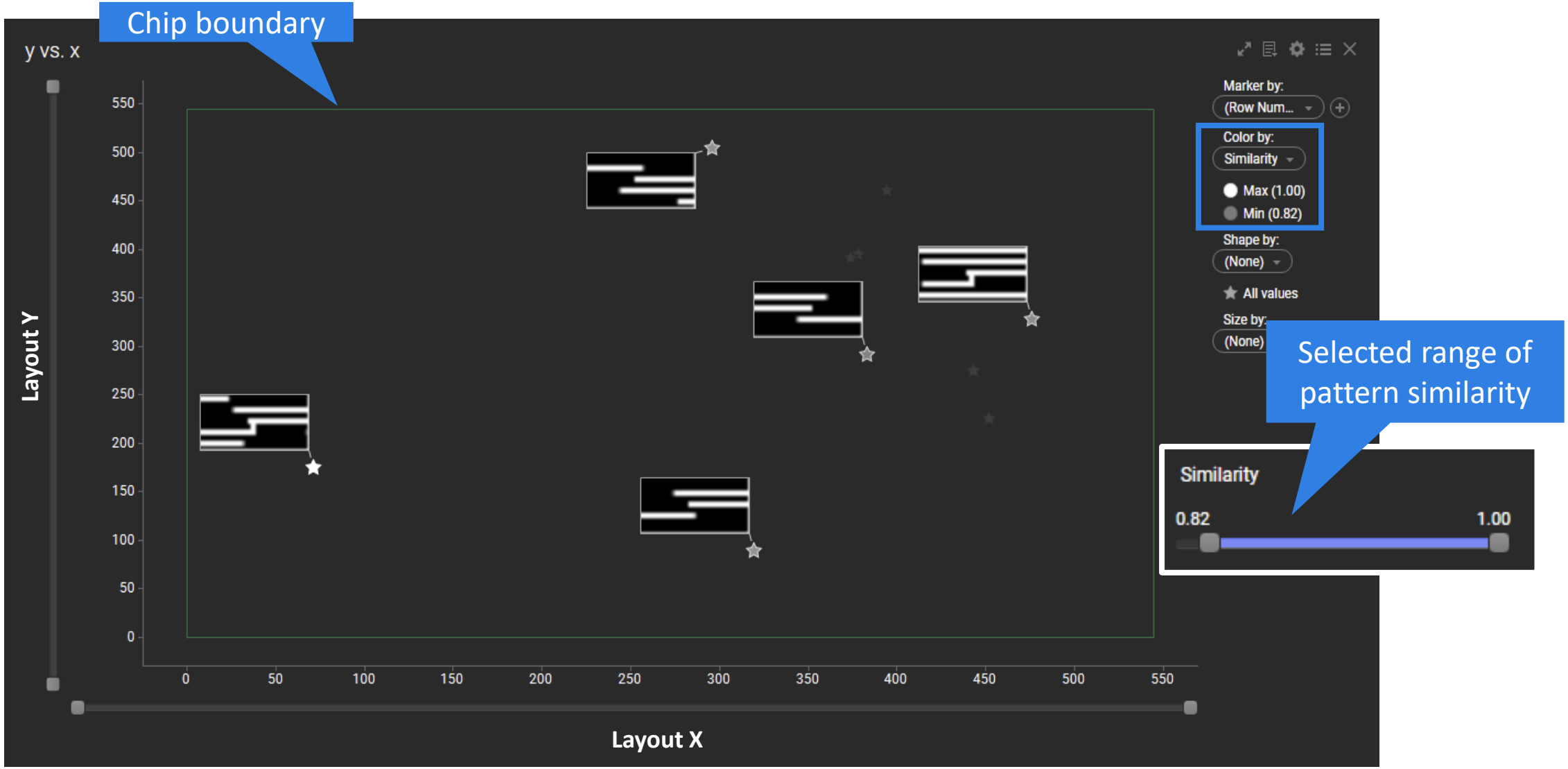
Full-chip

identification and localization

of groups of similar layout pattern systematics



Review spatial distribution of layout pattern candidates in Exensio

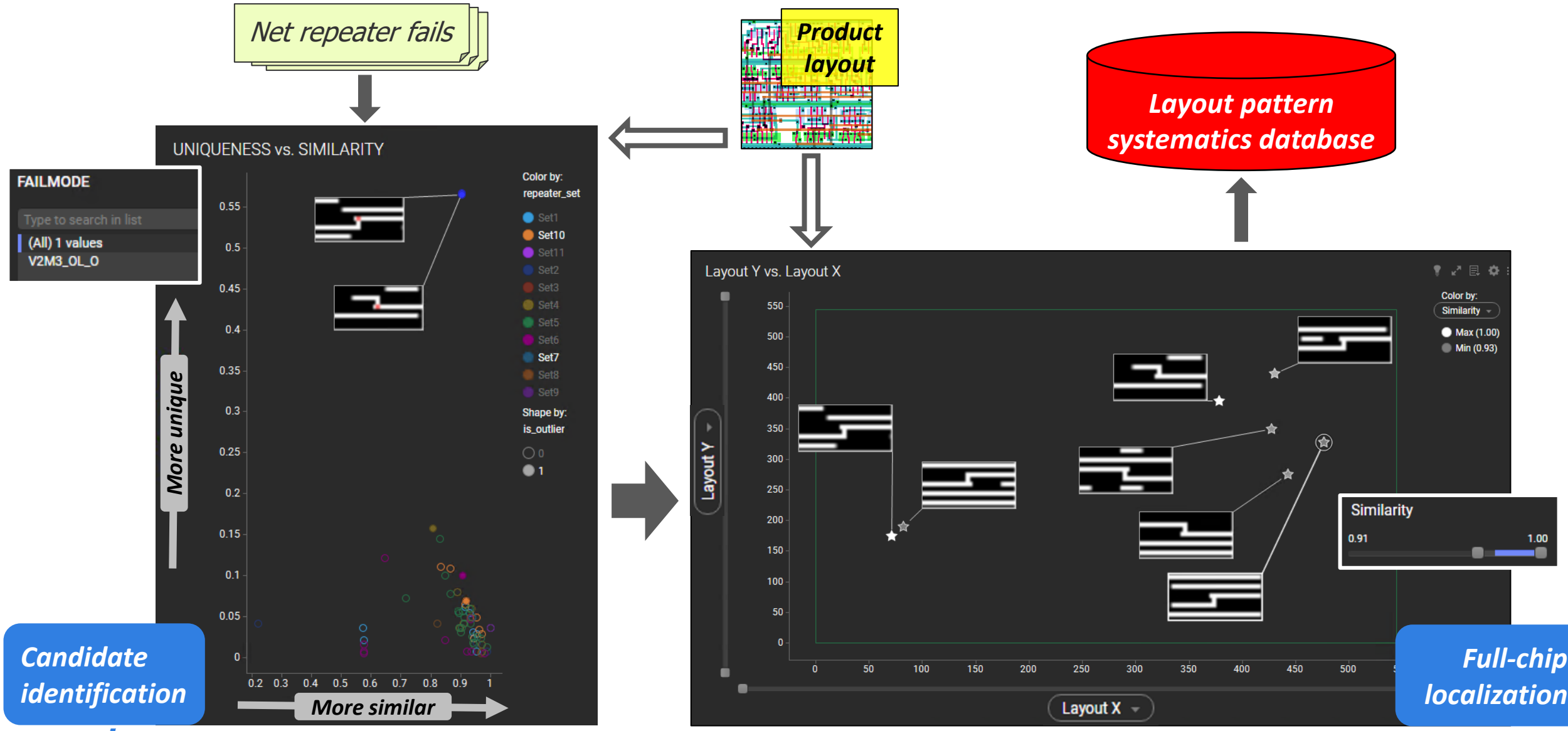


Similarity analysis

- Uniqueness and similarity analysis are both run across all layers
- Multiple layer interactions are also performed (such as VIA analysis)
- Analysis runs in hours even for large designs
- Volume scan diagnosis data of 2 to 4 lots is sufficient for analysis

Layout pattern systematics learning

Patent pending

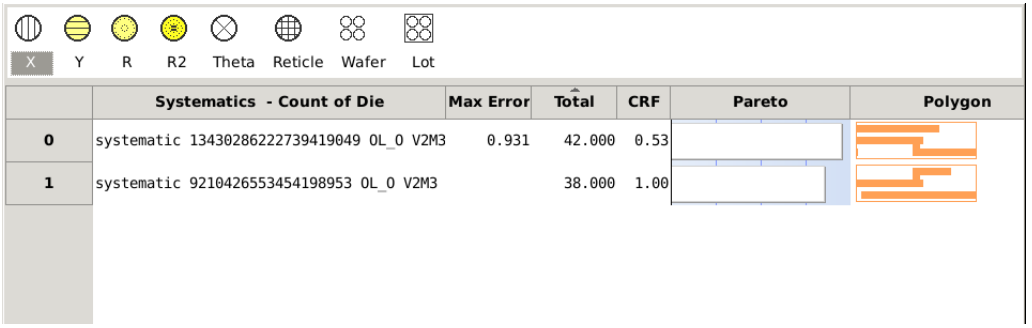


PDF/SOLUTIONS™ SIEMENS

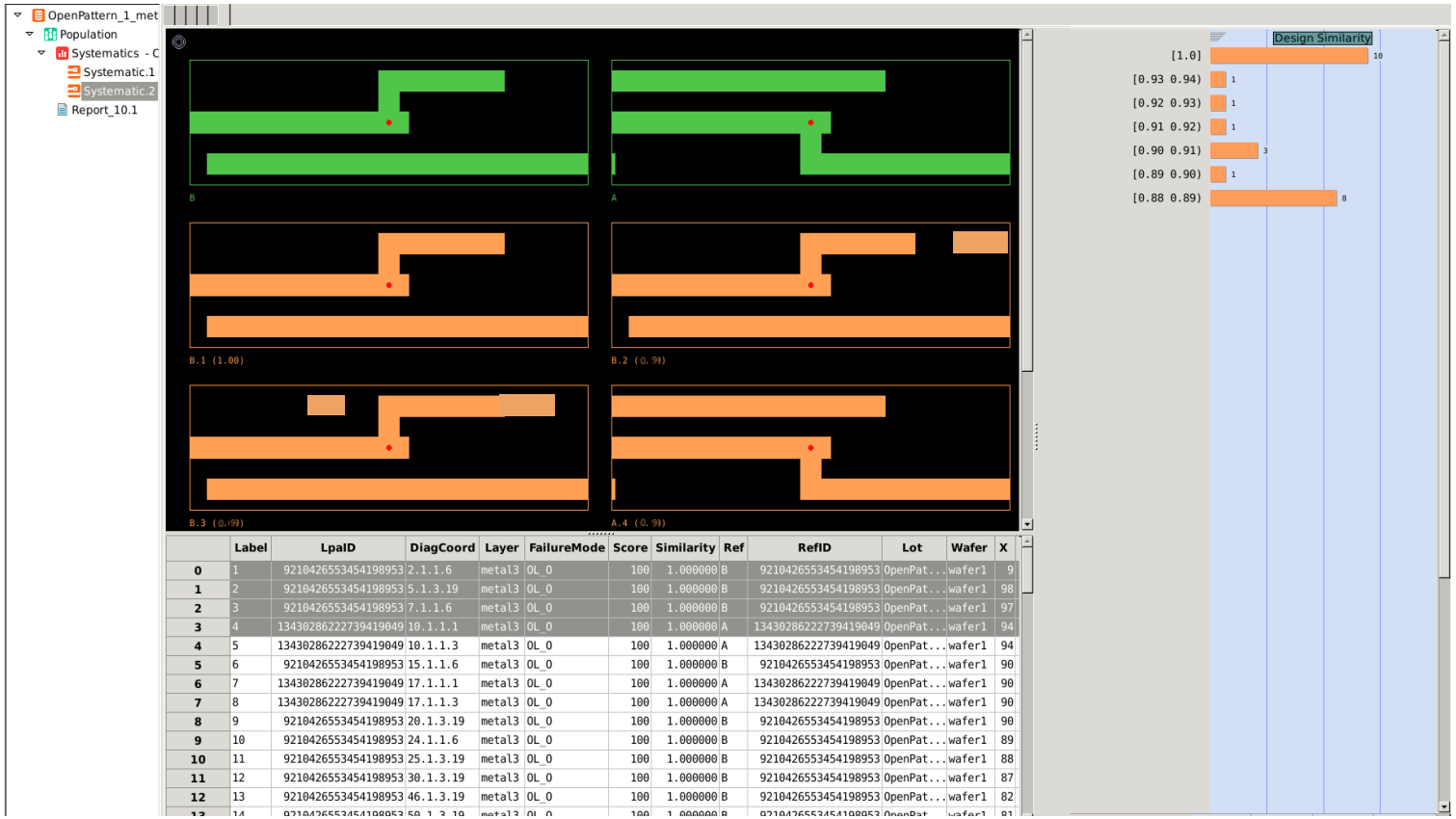
Patent pending

Overlay on diagnosis reports in Tessent YieldInsight

- Pattern gallery to analyze similar patterns in one place



	Systematics - Count of Die	Max Error	Total	CRF	Pareto	Polygon
0	systematic 13430286222739419049 OL_O V2M3	0.931	42.000	0.53		
1	systematic 9210426553454198953 OL_O V2M3		38.000	1.00		



	Label	LpaID	DiagCoord	Layer	FailureMode	Score	Similarity	Ref	RefID	Lot	Wafer	X
0	1	9210426553454198953	2.1.1.6	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	9
1	2	9210426553454198953	5.1.3.19	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	98
2	3	9210426553454198953	7.1.1.6	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	97
3	4	13430286222739419049	10.1.1.1	metal3	OL_O	100	1.000000	A	13430286222739419049	OpenPat...	wafer1	94
4	5	13430286222739419049	10.1.1.3	metal3	OL_O	100	1.000000	A	13430286222739419049	OpenPat...	wafer1	94
5	6	9210426553454198953	15.1.1.6	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	90
6	7	13430286222739419049	17.1.1.1	metal3	OL_O	100	1.000000	A	13430286222739419049	OpenPat...	wafer1	90
7	8	13430286222739419049	17.1.1.3	metal3	OL_O	100	1.000000	A	13430286222739419049	OpenPat...	wafer1	90
8	9	9210426553454198953	20.1.3.19	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	90
9	10	9210426553454198953	24.1.1.6	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	89
10	11	9210426553454198953	25.1.3.19	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	88
11	12	9210426553454198953	30.1.3.19	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	87
12	13	9210426553454198953	46.1.3.19	metal3	OL_O	100	1.000000	B	9210426553454198953	OpenPat...	wafer1	82

Patent pending

Volume scan diagnosis with layout pattern systematics

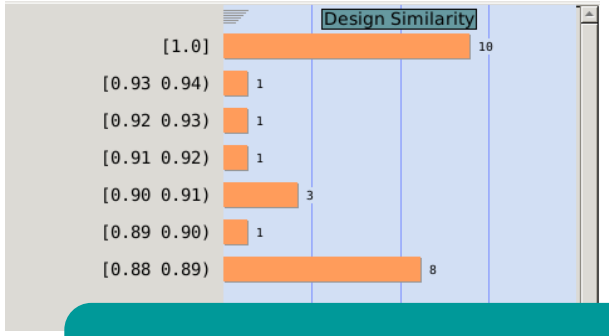
Diagnosis reports

Layout pattern systematics database

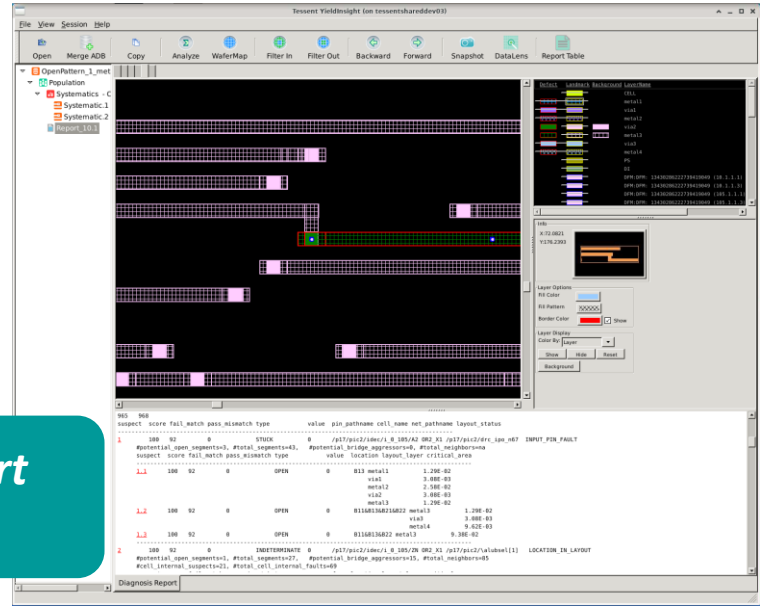
Annotate diagnosis population with layout pattern systematics

FA selection

Pattern gallery



Pattern similarity in diagnosis population



Review diagnosis report and layout context

PDF/SOLUTIONS™ SIEMENS

Silicon Results

- Successful demonstration on silicon dataset comprising multiple lots/wafers of scan diagnosis data with foundry confirmed layout systematics
- **Via opens in two lower metal layers identified as root causes of repeater fails**
- **88% of repeater sets attributed to the same two root causes confirmed by FA**
  - 2 repeater sets had other root causes
- **<10 layout patterns per repeater set identified for visual inspection (7X reduction in patterns to be inspected)**
  - ~65% of repeaters reduced to <=6 patterns for inspection
- **Ongoing live silicon engagements with mutual customers on advanced process node**

Key takeaways

- **FA today**
  - 2 or 3 PFAs confirming suspected systematic defect location
  - PFA is a destructive process that takes weeks
    - Pre cursor to PFA: ATE → Fault isolation ~3-6 weeks per part
  - Failure analysis (FI+PFA) costs $50-100k not accounting for engineering time
  - Time to confirm yield issue in PFA and apply corrective action is iterative >4 Months
- **This approach**
  - Isolation of PFA search area to high confidence locations
  - Reduce time for PFA and total number of PFAs for layout pattern systematics
  - Improve productivity and quality by making efficient use of FA resources

Overall value

- Current results demonstrate that identifying layout pattern systematics can be done accurately using scan diagnosis data and layout analysis from FIRE
- Reduced need for FI and FA can further enhance value of this solution for advanced nodes beyond 5nm
- Leverages design information at fabless to improve time-to-market in an increasingly demanding semiconductor market

Thank you!