PDF/SOLUTIONS™

2023 PDF Users Conference:

AI for tomorrow's manufacturing and R&D

Santa Clara Marriott - 2700 Mission College Boulevard Santa Clara, California 95054 USA

Helping to close the skills gap – PDF University

24th October 2023

Situational Analysis

- Chips Act(s) are being enacted around the world bringing advanced manufacturing into new regions.
- Graduating engineers have very little training on IC manufacturing data
- Newly announced fabs are targeted to be foundries, handling many different chips instead of integrated device manufacturers (IDM) that build just a few chip designs
- Manufacturers internal systems and software are not modern nor applicable globally:
  - Many separate databases: All Silo'ed
  - 80% of engineers time spent on data wrangling
  - Require deep domain-specific knowledge
- Engineers need software manufacturing analytics tools and methods that enable them to be more productive at geographically distributed foundries

Global Investments in Semiconductor Manufacturing

Investment programs to strengthen the semiconductor industry

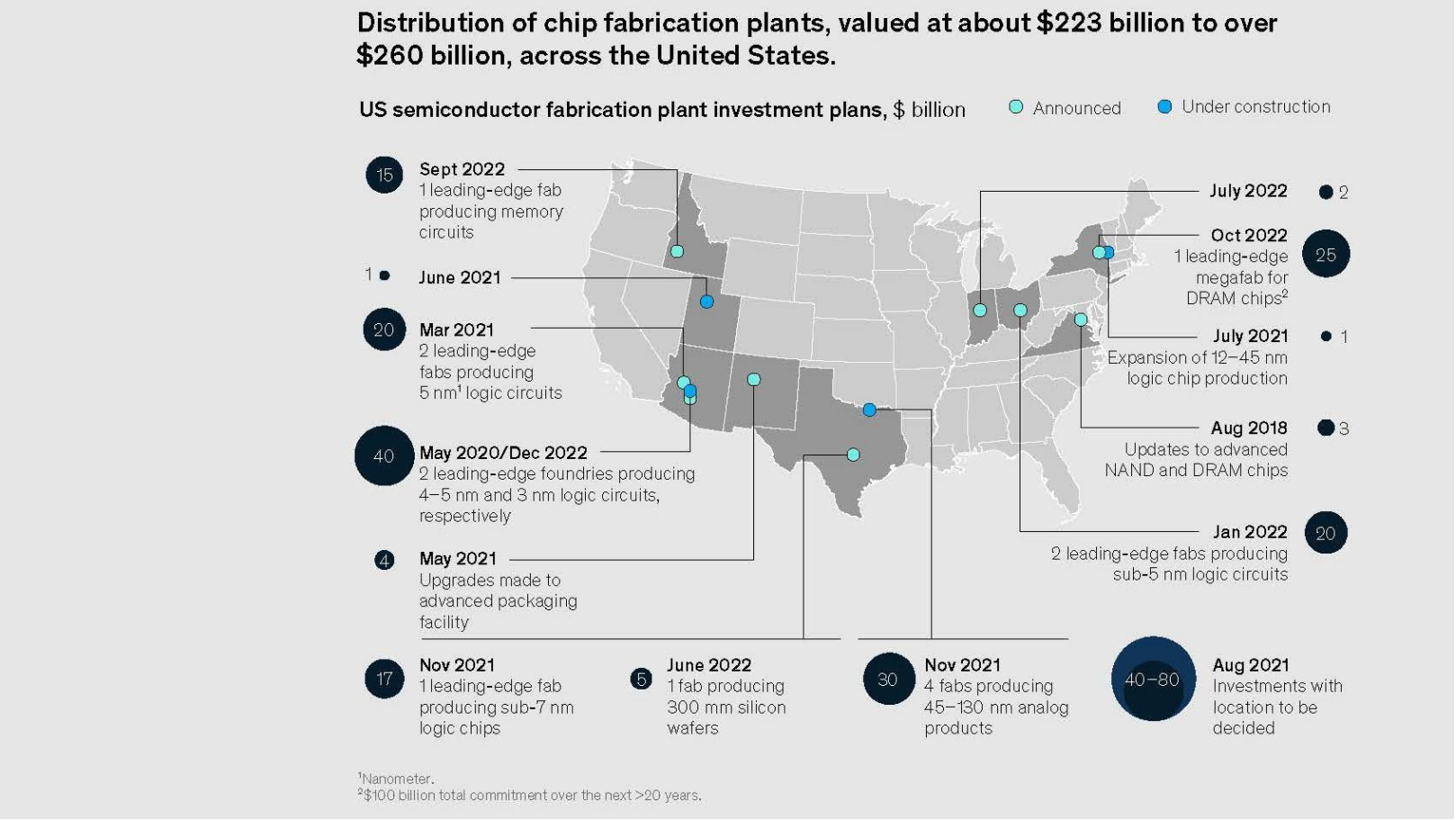
AS OF OCT 2022

NA/USA	Europe	Mainland China	South Korea	Japan
CHIPS For America Act	**European Chips Act**	**Made in China 2025**	**K-Belt**	**5G Promotion & NEDO Act**
Independence and technology leadership	Sovereignty and independence of the European chip industry	100% self-sufficient Chinese semiconductor industry by 2030	Independence (increase local content to 50% by 2030) and technology leadership	Drive growth in the national chip industry
$50 bn budget to promote the US semiconductor industry	**$41.7 bn** Estimated policy driven investment	**>$100 bn** Expected capital expenditure by National IC fund and regional government funds	**$240 bn** Corporate investments (2022-26) supported e.g., by tax breaks	**$5 bn** Budget to support advanced semiconductor manufacturers

Source: SIA; IHS; European Union; Press; McKinsey

McKinsey & Company 6

US Investments in Semiconductor Manufacturing



- Most existing Fabs in US, EU and Japan are IDM's; Now most new fabs are Foundries
- Advanced analytics skills are required to handle multiple products ramp-up and volume manufacturing

- Distributed workforce
- New locations in the areas without historically strong semiconductor industry/workforce
- Hard to build skills in one area

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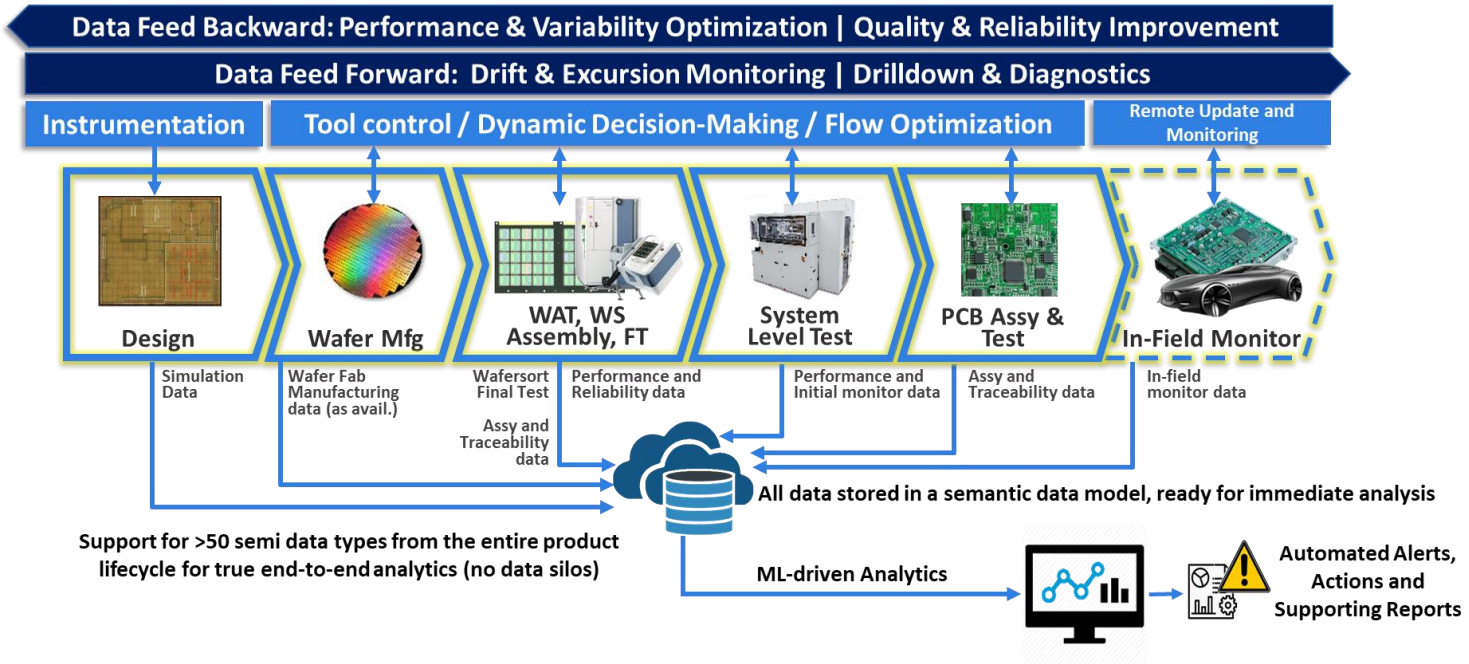
Analytics used to disrupt industries before

- Silicon Valley's approach to advertising was to bring real time analytics to the problem
- Created multi-trillion dollar market cap companies, larger than the entire ad industry before

- Similar approach is possible for semiconductor industry

- It cannot be accomplished with a 30 year-old software
- New generation employees will demand new efficient advanced analytics deploying AI/ML approaches

Exensio® Analytics Platform



- End-to-End Data Analytics for the Entire Semiconductor Product Lifecycle Management is required
- Training new generation employees to cover the entire spectrum is a demanding task

Revived student interest in the semiconductor industry jobs

- AI/Machine learning, cloud computing have been extremely popular courses especially for the MS students
- Most students lack understanding of Semiconductor industry
- Chip Acts created a new excitement and promise for lots of new job openings
- So huge opportunity to attract these students to the modern analytics/ML applications in semiconductor industry

First Implementation: MS-Level Class at CMU

- Provide Exensio on the private AWS Cloud
- Create challenging use cases where students solve real problems in small teams
- Exensio data analytics deployed to arrive at solutions
  - The ML Modeling Pipeline is not provided to the students
  - Make the projects challenging
  - Promotes coming up with original creative solution
- ML model development for sanitized real data from PDF Virtual IDM and Intel
- Award the winning team a prize ($500-1k)

First Implementation: MS-Level Class at CMU

- CMU customization:
  - Most MS students are already AI/ML savvy (either took the ML class or are taking it concurrently)
- However, weak semiconductor background
- Goal, while the focus is on ML, provide necessary backgrounds for the context:
  - Process Flow, Equipment, Device Architecture & Performance, SOC Components
  - Hardware for AI, Testing, Assembly including 3DHI
- Realistic Data Sets from **Intel**
- **Intel** participation: 3 Guest Lecturers
- **Many thanks to Dr. Sanjay Natarajan and his staff at Intel for their key contributions to the CMU course**

Project 1

- Data set: PDF's Virtual IDM based on historical data from an IDM customer
- Goal:Identify a subset of features that impact the Gate Critical Dimension (CD), i.e., the transistor gate length
- Employ various ML models such as Linear Regression, Random Forest, Decision Trees, and XG Boost, alongside with Analysis of Variance (ANOVA)
- Students explored Exensio ML offerings and compared the effectiveness of different methods
- ANOVA was the most efficient analysis method to identify the key equipment sensor parameters

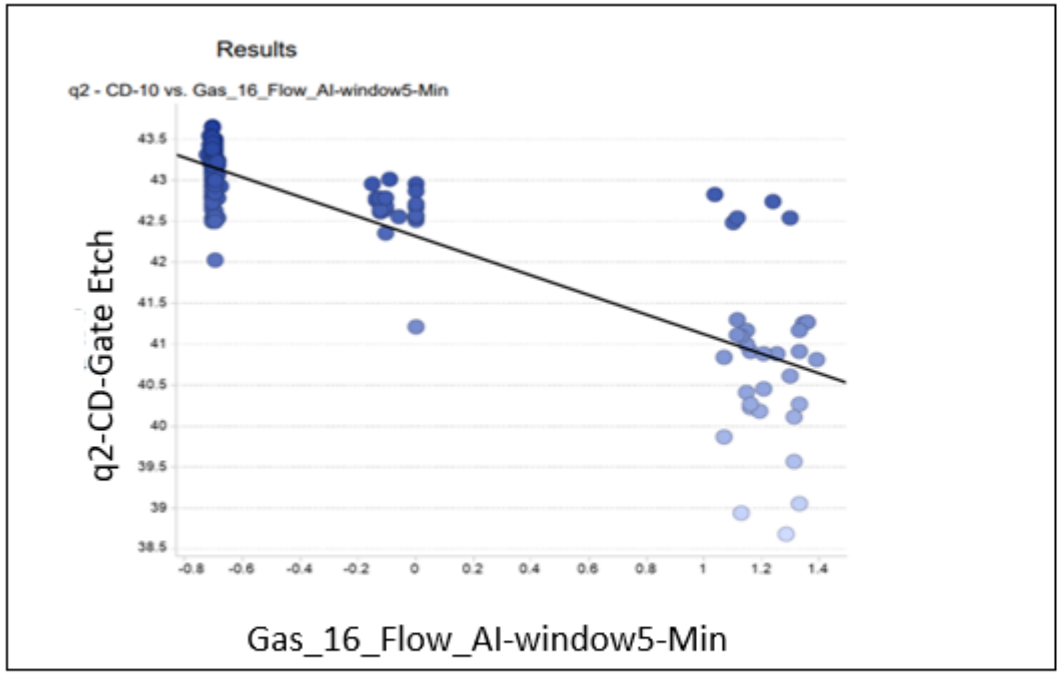


Figure 1 – Results using Linear Regression Model

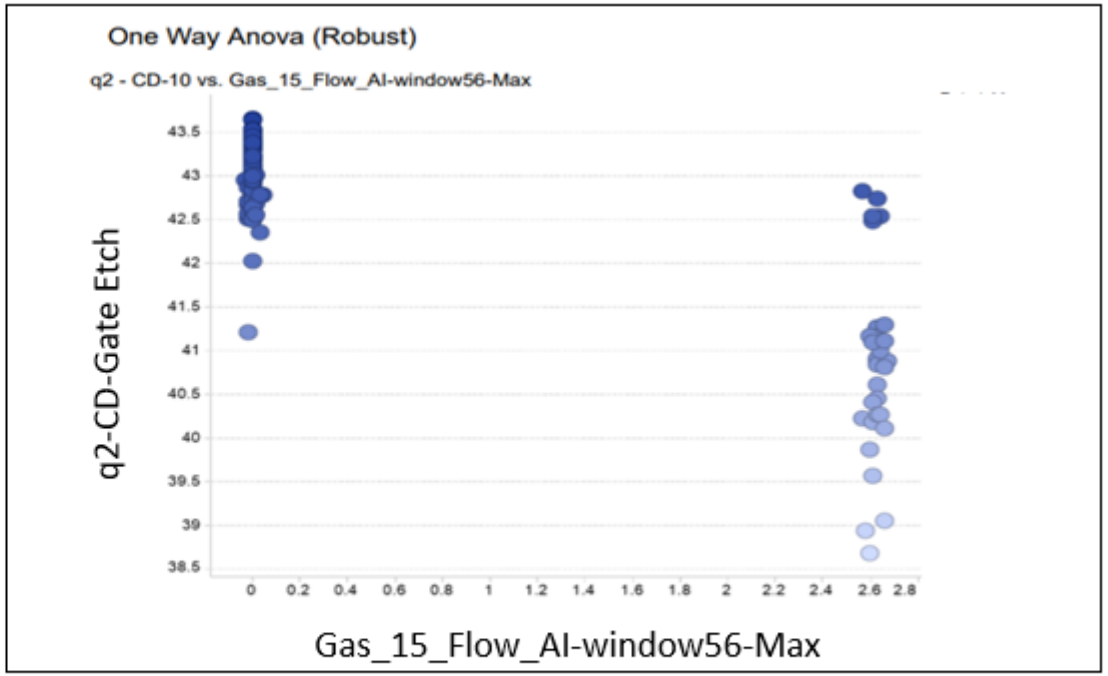


Figure 2 – Results using ANOVA

Project 2

- Data set: PDF's Virtual IDM based on historical data from an IDM customer
  - Fault Detection Classification (FDC) from the Scanner equipment real time n-situ sensos, Trace data from the Anneal equipment sensors, E-Test, Metrology and Wafer Sort Yield.
- Goal: Identify the key FDC parameters causing the yield loss and IDDQ by performing root cause analysis and building predictive models for yield and IDDQ.
- Students are really excited to work with real data
- They appreciate now how much the data pre-processing and datamining must happen before the ML model building to succeed

Project 2 Insights

- The direct attempts to build the predictive models in ChatGPT failed to identify the key FDC indicators
- The winning approach:
  - Recognize that the yield losses were mostly at wafer edges by using Exensio's spatial (zonal) analysis
  - Spatial analysis on the Wafer Sort and Metrology data
  - Build hierarchical models (YA-FDC methodology in Exensio): Metrology/Misalignment Yield loss & IDDQ & FDC Metrology
  - The final stage is to build a predictive model for yield loss and IDDQ using built-in Exensio ML approaches that they learned in Project 1
- Make sure that the models are not overfitted by employing the appropriate training, testing and cross-validation methodology

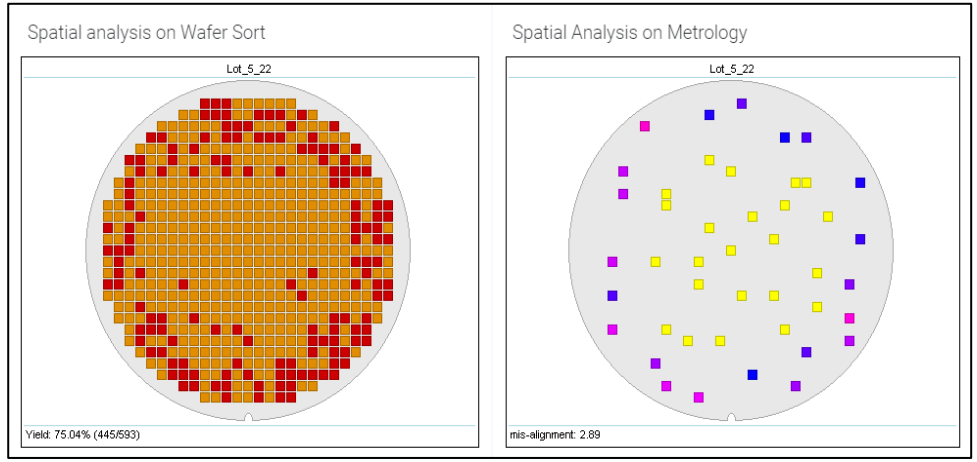


Figure 1 – Spatial Analysis on Wafer Sort and Metrology

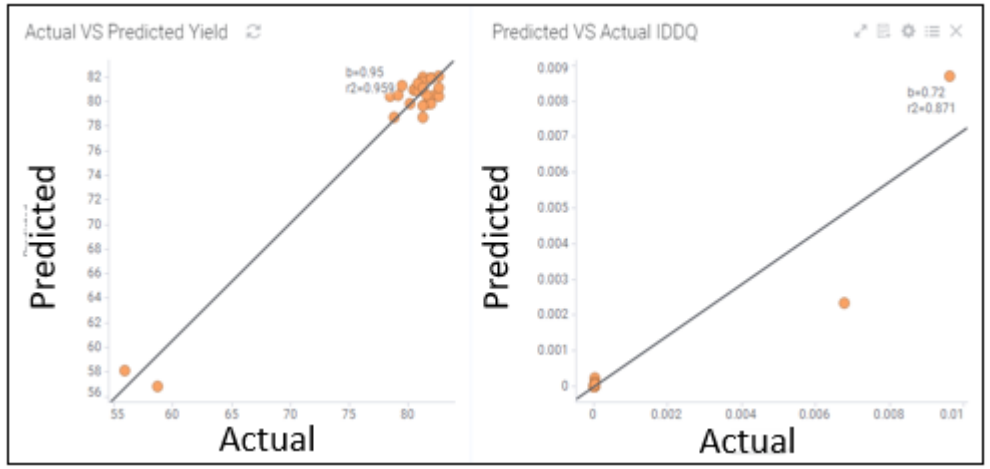


Figure 2 – Model Performance for Yield and IDDQ

Project 3

- Intel data set: Sanitized data from a real product
- Goal: Identify failed Bins from two types of Bin data and analyze yield degradation over time by performing root cause analysis for the identified bin excursions for the Wafer Sort and Final (Class) yield data.
- The primary objective is to identify a significant set of operations (groups) that contribute to excursions in Yield/Test bin signals and identify the time stamps for these excursions.

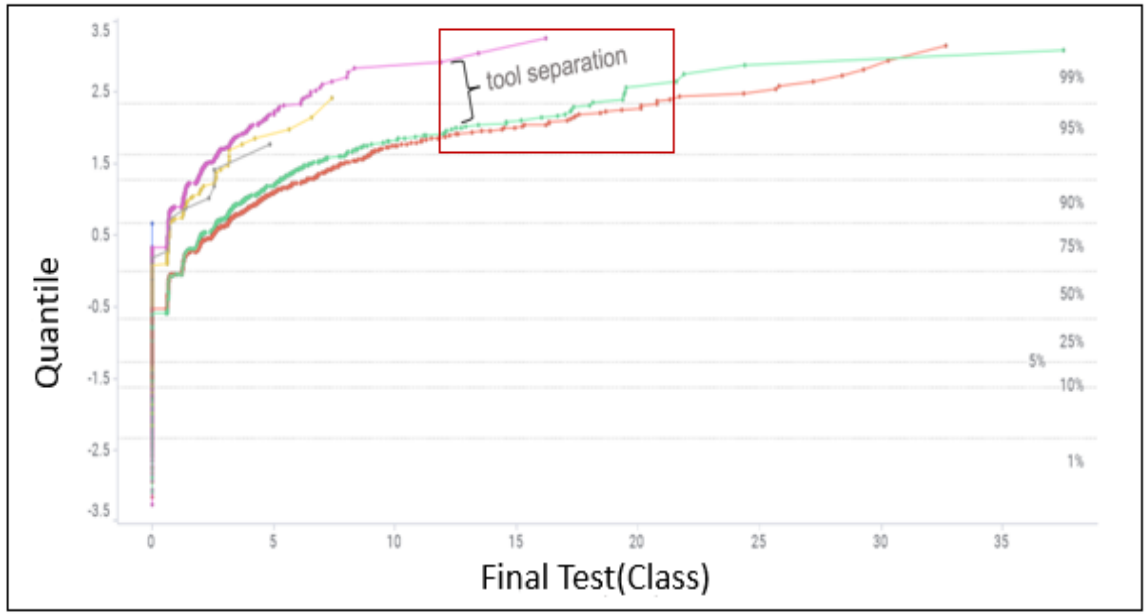


Figure 1 – NQP plot for detecting tool separation over Final Test

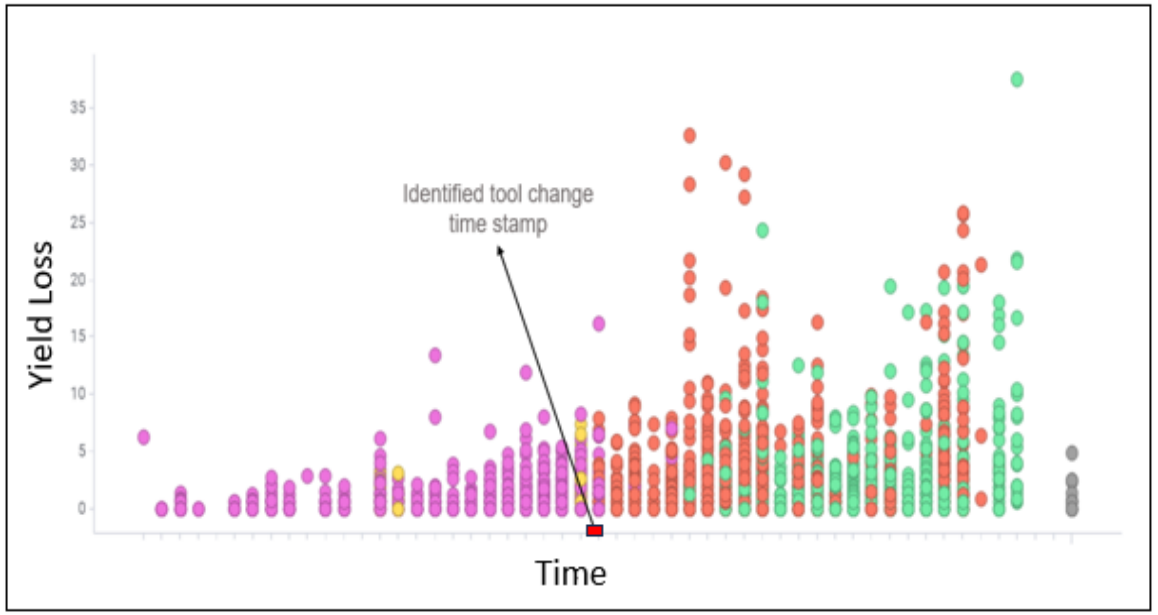
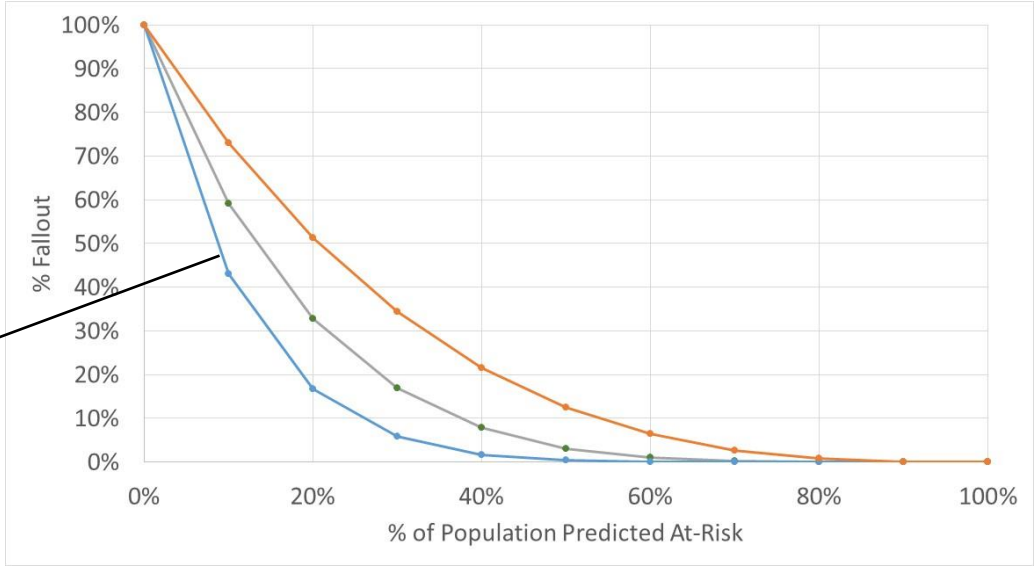


Figure 2 – Tool identification for yield loss over time.

Project 4

- Intel data set: Sanitized data from a real product
  - This project involves data from the product which consists of two die in a package
  - Data set: Wafer Sort & Final (Class) Test data
- The primary objective to utilize ML Modeling Pipeline in Exensio for screening a vast dataset with 17k Wafer Sort parameters and 500k records (almost 200 GB of uncompressed data)
- Develop a predictive machine learning model for screening of die based on Wafer Sort test data to minimize the cost associated with assembling defective dies and rejecting the good ones.

Best Model



Student feedback to date *(Projects 1 & 2 Completed, Project 3 underway)*

- Interesting real data projects related to the lectures

- Exensio Feedback:
  - Valuable datamining and pre-processing techniques
  - Good applications of ML model development and validation
  - Good support for screening, ML modeling and ANOVA
  - Excellent visualization of data prep analytics and final results

Future Plans for the Analytics Courses

- Course can be expanded to more use cases contingent on available data sets. Participation opportunities for sponsoring companies in syllabus & data
- Intel and PDF are planning to expand the class beyond CMU:
  - Arizona State, Ohio State, Internal class for employees for professional certificates
- Other US companies
- Oustide US
  - Germany
  - Japan: corporations
  - Taiwan: universities
- Potential funding sources: Companies, Chip Acts (EWD in the ASIC Consortium), ME Commons (CA DREAMS), American Semiconductor Academy (SEMI & UCB – Prof. Tsu-Jae King Liu)
- **Class content and especially projects need to be customized for each company/university**

Big Picture Goals

- Develop workforce who can use software to bring to scale what has been done in conventional foundries w/ human capital

- Develop a research community in the US that re-imagines analytics for fabs in the same way ad-tech was re-imagined
  - Wide data (not just one tool or one equipment company)
  - Real-time
  - Personalized for each product

➢ **Scale foundries, test and product engineering for the 21st Century**