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2023 PDF Users Conference:

AI for tomorrow's manufacturing and R&D

Santa Clara Marriott - 2700 Mission College Boulevard Santa Clara, California 95054 USA

Innovation Focus in Advanced Solutions

24th October 2023

Advanced Solutions Group



- Vision: To be the world's leading data and analytics platform spans the semiconductor and electronics ecosystems.
- Mission: Provide innovative solutions to create, access, and organize data to enable analysis and control for semiconductor and electronics companies to achieve better time-to-market, yields, quality, and operational efficiencies.

Advanced Solutions Group

- ASG develops new methods, tools, and applications to support PDF's vision
- Example innovations from ASG:





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Innovation Focus in Advanced Solutions

Using AI to connect Design, Test, and Analytics (DTA)

How to use design information to better drive test and yield diagnostics in Exensio? We are working on various AI algorithm to connect design to test and then to yield diagnostics, especially to address systematic fail modes.

• Our Generative AI: Generation of unique observation with help of AI

It is getting harder to "see" various fail modes in advanced nodes. We use AI to assist the design and measurement of some PDF unique elements to characterization of process & product that are hard to observe by traditional approach. Examples include LLE DOE, CV Core, and dScan-by-FIRE.

* Contents include a combination of existing solutions and future roadmap items

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2023-2024 R&D Roadmap to Connect Design – Test – Analytics



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Exensio FIRE Software: Fuzzy Pattern Al

A given systematic fail mode usually comes from, not one, but a "family" of layout configurations. Traditional rule-based approach is insufficient for the evolving complexity of product design at advanced nodes



Using fuzzy pattern classification algorithm, PDF's Exensio FIRE software automatically groups all similar patterns of same fail mode into a "pattern family".



"How to Classify Photos of Dogs and Cats (with 97% accuracy)" -- machinelearningmastery.com © 2023 PDF Solutions, Inc.

Pug Dog breed :

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PDF Solutions and Siemens EDA accelerating yield



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Siemens EDA's Tessent Diagnosis/YieldInsight + PDF's Exensio/FIRE

enabling diagnosis of systematic yield loss

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Tessent and Exensio/FIRE working together

Approach: *Similarity vs Uniqueness*



Customer Benefit

For a product in production at advanced node:

- 7x improvement in inspection and/or PFA efficiency
- By identifying root causes for ~90% of measured failure
- Coming from lower layer and upper layer metals

ModelOps and Edge Inference for Test

How ModelOps increases Business Value

Lifecycle Management, Monitoring, Control and Operationalization of AI /ML / decision models



Day 2 Technical Presentations

 Operationalizing and Scaling AI/ML for the Semiconductor Industry, by Jeff David

 Edge Inference for Test, by Greg Prewitt

Shifting from Model-Centric to Data-Centric Al

Conventional model-centric approach:





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Credit: **Andrew Ng**, NeurIPS Workshop, Data Centric AI, December 2021 Example of data movement for a model for Final Test:

- Data from Fab
- DFF (Data Feed Forward) of outcome of fab predict model from above
- Data from wafer sort
- DFF of outcome of WS model from above
- (more complexity for multi-chip solution)

PDF's ModelOps pipeline takes care of the complex issues related to data collection, alignment, feature extraction, DFF, validation, corner event treatment, etc, and is integrated with facilities' MES.

AI/ML for Testing Optimization, but ...

Current Approach





AI/ML for Testing Optimization, but ...

Current Approach Use Information from Design Exensio FIRE NEW **Optimize Test Run Many** Based on "DNA" Wafers 1111 PMO **Understand "DNA"** within the Design 3 **Deploy Model Build The** Update the "Understanding" **On Tester** Model as More Test Are Cumulated

Dealing with Many Product Tape-outs

Product A



Problem

of products > # of employees

Dealing with Many Product Tape-outs





Enable cross product applications

- E.g. identify common low yielding IP across products
- E.g. common systematic yield loss across products
- E.g. to update "importance" of each gene from existing product to new product introduction

2023-2024 R&D Roadmap to Connect Design – Test – Analytics





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Use Generative AI to Design CV TestChip: LLE example

Characterization of local layout effect is critical for products at advanced nodes.



Fig. 5. Example layout patterns for characterizing layout effects: (a) Polypitch-induced variation due the to impact of lithography and stress, (b) activeextension-induced variation due to STI stress, and (c) gate-poly-shape-induced variation due to corner rounding.

Variation in Transistor Performance and Leakage in Nanometer-Scale Technologies; IEEE Transactions on Electron Devices, Vol. 55, No. 1, January 2008

- Traditional approach requires more silicon area than physically possible to characterize all behavior.
- Using AI algorithm, PDF can select and create a small set of fundamental components (we call pixels) that represents all LLE effects.



Large and Effective Dataset is needed to Train AI Algorithm

To train Generative AI algorithm for test chip design, large and effective dataset is needed, as also being recognized in the industry.

Si	Authors		
A Collaborative Data Model for Al/ML in EDA	Kerim Kalafala, IBM		
Artificial Intelligence, Classification, EDA, Machine Learning, Standards	Veeravanallur Parthasarathy, AMD		
This work explores industry perspectives on:	Norman Chang, ANSYS		
1. Machine Learning and IC Design	Akhilesh Kumar, ANSYS		
2. Demand for Data			
3. Structure of a Data Model	Elias Fallon, Cadence Design Systems		
4. A Unified Data Model: Digital and Analog examples	Sriram Madhavan, GLOBALEOUNDRIES		
5. Definition and Characteristics of Derived Data for ML Applications	Shran Madhavan, GEOBAEI CONDINES		
6. Need for IP Protection	Prateek Bhansali, Intel Corporation		
7. Unique Requirements for Inferencing Models	Sripiyas Podapati Intel Corporation		
8. Key Analysis Domains	Similar Bodapati, inter corporation		
9. Conclusions and Proposed Future Work	Chandramouli Kashyap, Intel Corporation		
Abstract	James Masters, Intel Corporation		
A standard, common method for classification and structure of machine learning training a interoperability is critical to enable and accelerate the use of artificial intelligence and mach	Ramy Iskander, Intento Design		
electronic design automation. Subject matter experts from across the semiconductor and i	Larg Weiland, PDF Solutions		
including digital, analog, shapes-based and IP development. The authors conclude that in o	Karthik Aadithya, Sandia National Laboratory		
applications for EDA, a collaborative and coordinated approach is needed. A prerequisite fo the best process for organizing, leveraging and sharing data. Si2 industry survey results sho	Boon-Siang Cheah, Synopsys		
organization for Al/ML data in EDA. A common data model would address the data organiz EDA tool developers, IP providers and researchers by first supporting the high interest EDA	Mengdi He, Synopsys		
derived data.	Leigh Anne Clevenger, Si2		

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- As the largest independent commercial characterization test chip provider, only PDF's dataset has:
 - hundreds CV test chip for FinFET technologies
 - Up to **1 billion** of DUT per CV test chip design
 - More than **100,000 wafers per year** tested using PDF's pdFasTest tester

Example Whitepapers: at Silicon Integration Initiative (Si2) https://si2.org/ai-ml-downloads/

CV Core Sensor for Reliability and 3DHI



Using AI/ML on CV Core data for Burn-In Optimization

CV Core data based AI model for lookahead prediction (e.g. Wafer Sort to Final Test):
20X improvement of capture rate for burn-in optimization

Traditional Inking		CV Core based Prediction $f(x)$			
Overkill budget: 0.019 Capture rate: 0.0%	%		Overkill budget: 0.02 Capture rate: 19%	1% = (# predicted fail b 6 = (# predicted fail th	ut actual pass) / total nat actual fail) / # act
# of die	Predicted fail	Predicted pass	# of die	Predicted fail	Predicted pass
Actual fail	0	YY,000	Actual fail	Z',000	YY',000
Actual pass	0	XXX,000	Actual pass	AA	XXX',000
Overkill budget: 1.0% Capture rate: 2.3%			Overkill budget: 1.09 Capture rate: 52%	%	
# of die	Predicted fail	Predicted pass	# of die	Predicted fail	Predicted pass
Actual fail	Z,000	YY,000	Actual fail	ZZ',000	YY',000
Actual pass	A,000	XXX,000	Actual pass	A,000	XXX',000



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at 3nm/4nm

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PDF developed DFI eProbe to address this challenge.

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DUT Density (M/mm2)

2.3

Exensio FIRE to Drive More Efficient Inline eBeam Inspection

FIRE AI algorithm summarize design geometrical, electrical, and expected ebeam characteristics, to enable selection of scan points, to take advantage of HW vector scan capability.



- FIRE created eProbe inspection recipe leads to 10-100X efficiency gain for systematic fail mode measurement.
 - Example: eProbe-350 on N7 logic block





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Example Workflow to Shorten Learning Cycle

For subsequent tape-out, inspection recipe can be created at/before tape-out to assist NPI.

Direct inline inspections of all locations of this systematic fail mode



For a given product, FIRE extract all (x,y) locations of this systematic fail mode, and create recipe to drive DirectScan™.

The layout attribute is "tagged" with each location, which allows us to study the relationship of failure with layout attribute (process margin).

Example one family of fuzzy pattern











AI Related Roadmap of PDF Advanced Solution

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AI Related Solutions from ASG

Available NOW

- Siemens Tessent + PDF Exensio/FIRE integrated solution for scan diagnostics
- Exensio Test with ModelOps
- CV Core sensors and related apps
- − DirectScanTM eProbe with Exensio FIRE

On Deck

- ATPG + Exensio FIRE using design DNA
- PLM + Exensio across multi-products
- Generative AI for CV test chip design

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