End-to-End Yield Management for Compound Semiconductors Manufacturing

Steve Zamek[1*], Dave Huntley[1], Jon Holt[1]
[1]PDF Solutions Inc, 2858 De La Cruz Blvd., Santa Clara, CA 95050 USA; *E-mail: steve.zamek@pdf.com

Keywords: Compound Semiconductors, Silicon Carbide, Manufacturing Analytics, Process Control, Yield Management

Abstract

Progress in Compound Semiconductors is hindered by the high level of defectivity of the initial material. Here we take Silicon Carbide manufacturing technology as an example and provide an overview of manufacturing analytics tools and methodologies used to drive yield ramp and capacity expansion. We focus on 2 examples of site-to-site handoff: substrates handoff to IC front-end fab or foundry and wafer hand-off to the assembly and test site. Holistic end-to-end yield management is enabled by deploying Big Data platform at the enterprise level. This framework applies to both fabless companies and IDM's. It also extends to a fully outsourced, fully vertically integrated IDM and anything in between.

Introduction

As the SiC industry is transitioning from 150 to 200 mm based substrates, manufacturers will continue facing challenges with yield management. While the competition in the SiC substrate space intensifies, companies are increasingly adopting advanced manufacturing analytics tools to increase efficiency and reduce cost. Luckily, the mature silicon IC industry developed such tools, and they can greatly accelerate learning.

In this article we review the best-known methods for analysis of defects and their impact on yield. These were gathered throughout the years as a result of data analytics deployments in major foundries, IDM's and fabless companies [1]. Here, we take Silicon Carbide (SiC) as an example due to its fast-growing adoption in the power IC market.

Typical manufacturing flow is shown in Figure 1 [2,3]. As opposed to silicon IC's, here the major cost drivers are the earlier steps in the process, from crystal growth out to epitaxial wafers. While the cost contribution from the material has been dropping, it is expected to remain in the range of 20 to 30% of the final product cost [4]. Tackling defectivity is quite challenging, since material defects undergo transformations during epitaxy and manifest themselves late in the manufacturing and test flow.

Understanding the true impact of material defects requires a holistic end-to-end (e2e) yield management at the enterprise level. However according to the 2024 survey [5], compound semiconductors and silicon carbide manufacturing in particular, is lagging far behind silicon. According to the report, "*most companies fail because they neglect to establish a solid data model foundation*".

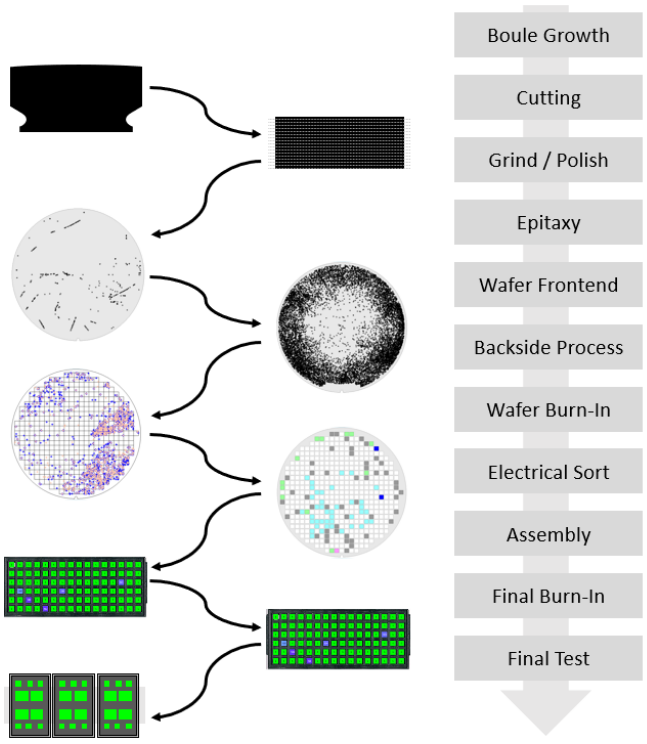

Fig. 1. Typical manufacturing flow for SiC

Big Data for Yield Management

It is the job of a Big Data platform to manage, process and analyze large volumes of structured, semi-structured, and unstructured data. Ultimately, the goal of analytics deployment is to understand what happened, why it happened, what will happen and take the necessary action to drive the desired outcome. Standardizing across many roles in the organization (design, operations, manufacturing) and across different sites (materials, IC front-end, assembly and test) on a single data platform enables breaking the data silos and streamlines collaboration. It facilitates accelerating yield ramp and helps avoiding yield crashes in time. Longer term, it also enables identification of yield bottlenecks in the entire manufacturing flow end-to-end. As opposed to point analytics solutions with a variety of disjoint tools, unified analytics platform offers optimum decisions at the enterprise level.

To illustrate this, Fig 2 provides a few examples where large volumes of post-epitaxy defect data are stacked at various levels and filtered by various attributes. The table explains at what level the data was stacked and what filtering was applied. Distinct spatial signatures become clearly visible, allowing identification of complex interactions between a particular substrate supplier and a particular epitaxy tool.

Analysis of Kill Ratios (KR), is common in mature silicon fabs [6]. Calculation of KR is based on die-level defect summaries as shown in Fig 3. Here "clean" and "dirty" categories are determined by optical inspection, while "pass" and "fail" are determined by the electrical test. However, implementation of such an analysis in compound semiconductor manufacturing has been challenging. It's helpful for: (1) ranking the manufacturing steps by their contribution to the yield, and (2) understanding the efficiency of defect inspection for yield and quality.

Challenges

Typical material flow is depicted in Fig 4. Dotted horizontal lines indicate material hand off. They can represent hand-offs between different companies, as is the case for the fabless-foundry model. They also represent the IDM model with full vertical manufacturing, since typically crystal growth, substrate manufacturing, front-end and assembly and test happen at different sites.

Many researchers examined the impact of defects on the electrical device characteristics [7-8]. However, implementing standard methodology to assess the true impact of defects for compound semi remains a challenge due to the following factors [9]:

- Complex material flow: frequent lot splits, reworks, and varying wafer ID's make wafer (substrate) traceability a challenge. This is illustrated in Fig 4.
- Siloed sites: data comes from multiple manufacturing sites (fabs, foundries, assembly and test facilities) and is typically missing key contextual meta data. This makes it difficult to align manufacturing data across multiple operations at the enterprise level.
- Multiple electrical test bin-maps merge operations are required to capture proper statistics of all failed die; this is far from trivial because some binmaps need to be reconstructed from the unit-level test data or final system-level burn-in.
- Nuisance defects: typical defect wafer maps include a very large number of defects per wafer. This dramatically skews the statistics as all dice appear to be defective.
- Inline inspections are done by multiple tools with inspection recipes not following the same conventions for defect class codes or class naming.
- Defect source analysis is challenging as during the epitaxy defects expand, shift and undergo transformations.
- Material traceability (both wafers and units) in both directions – upstream and downstream.

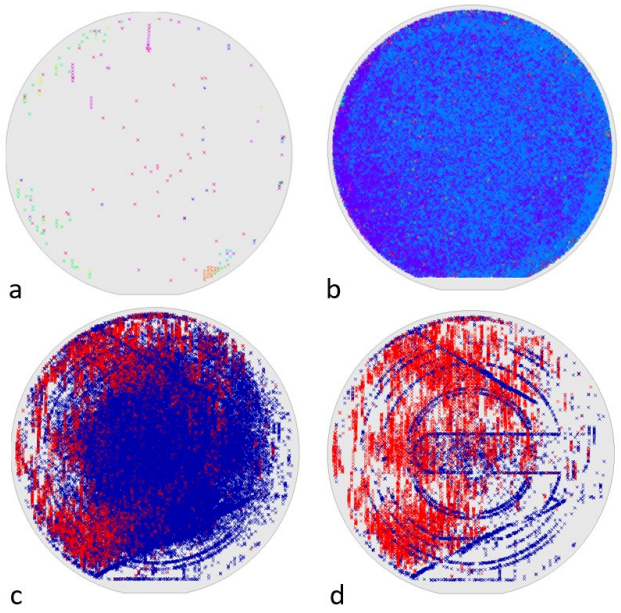

Fig. 2. Example of defects in SiC after epitaxy with various levels of data stacking and filtering

#	stacking by	filtering by
a	---	---
b	+epi product	---
c	+substrate supplier	+defect type
d	+epi reactor	+defect size

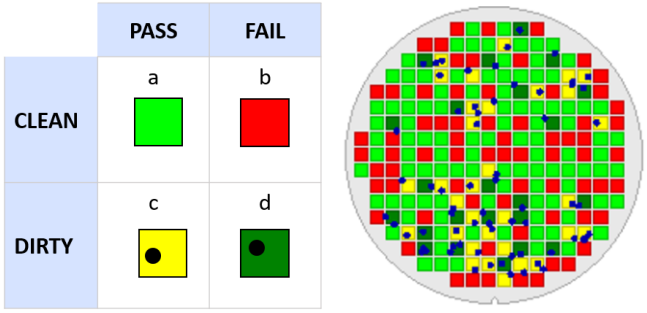

Fig. 3. Wafer-level defect summaries

Deployment of Analytics in an Enterprise

Fig 5 shows a typical deployment of YMS within the enterprise IT ecosystem. Such an ecosystem consists of many software tools including MES, ERP, EAC and more (with the acronyms defined at the end of this publication). It is the job

of the YMS to align all data across hundreds and thousands of manufacturing steps within the semantic data model.

In the compound semi world, many manufacturing sites run on a variety of different MES, FDC, SPC and YMS systems. This is true even within a particular IDM, since many IDM's utilize sites acquired via M&A process. Those sites have been running on their legacy SW systems with little to no cross-site commonality. To address the challenge, several IDM's adopted the architecture shown in Fig 5.

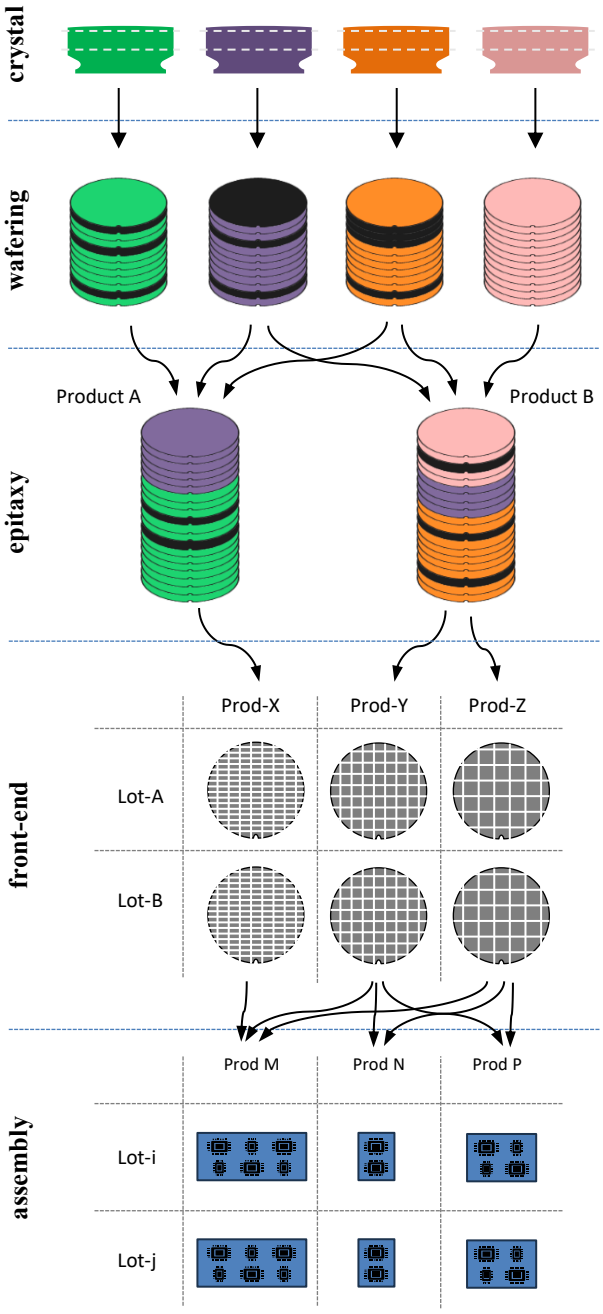

Fig. 4. Diagram of material flow (oversimplified)

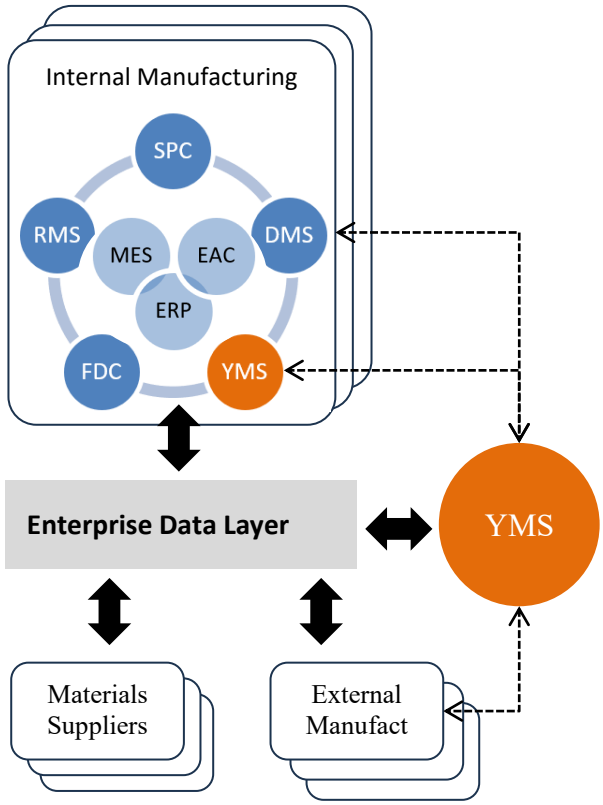

Fig. 5. Deployment of analytics and automation at the enterprise level (see acronyms below)

As shown, the Enterprise Data Layer serves to bring data from many sources to a common standard. Such a layer is a critical piece of the enterprise data strategy, as it simplifies e2e analytics and facilitates decision making. Nevertheless, even with the lack of such layer, several of our customers successfully deployed enterprise-wide YMS. Aside from the data standard, such a layer insures site-to-site consistency and traceability of substrates, wafers, dice and packages.

Traceability begins when the substrates are cut from the crystal where they receive their first ID. This is typically a virtual ID, since any physical marking will get removed during the grinding and the polishing process. Since compound wafers are processed in legacy silicon fabs, front-side wafer scribe is being used to track the wafers in the fab. However front-side scribe may compromise the epitaxy process, so backside scribe is preferred at steps leading up to the epitaxy. Bottom line, there are various reasons for virtual identifiers and front- and back-side scribes to be added throughout the wafering, epitaxy, front-end, and assembly steps. Tracking these ID changes provides a crucial to link back to the original crystal and is referred to as Wafer Level Traceability (WLT).

At assembly, dice are transferred to multi-die packages and modules where they undergo final burn-in and test. The challenge in SiC manufacturing is that testing at proper load

conditions (power and temperature) cannot be done until the final module is complete. Failures at final test may have been caused by a defect detected early in the process, but all the manufacturing costs must be incurred before the part can be scrapped.

To enable rapid learning, it's imperative to correlate the final test failures with earlier defects and the single device level. For this we need to precisely track the transfer of every device from wafer to package to module. This is referred to as Single Device Tracking (SDT) which depends heavily on a common semantic data model provided the SEMI E142 industry standard [10,11].

While many SiC manufacturers struggle with traceability, these challenges are not unique to compound semiconductors. Mature silicon industry is assembling many dice from a variety of suppliers into single modules. Examples of such integration are compute modules for datacenters, which contain dozens of chiplets for logic (CPU and GPU), memory (DRAM and HBM), and IO. In many of our current YMS deployments, the traceability ownership is shared between us (the YMS provider) and the enterprise data layer.

SUMMARY

Compound semiconductor manufacturing is lagging behind the mature silicon industry in adoption of analytics and automation. Challenges are numerous, but tools and methods developed in traditional silicon manufacturing are here to help. Here we presented end-to-end yield management platform and discussed deployment strategies thereof. Such a platform enables manufacturers to assess the end-to-end impact of material defects and make educated decisions. While the discussion here focused on SiC, majority of the statements apply equally well to the broader compound semiconductor industry, including GaN, GaAs, InP, and more. Examples provided in this article are based on numerous deployments across broad customer base.

ACRONYMS

AEC	Equipment Automation and Control
DMS	Defect Management System
ERP	Enterprise Resource Planning
HBM	High Bandwidth Memory
KR	Kill Ratio
M&A	Mergers and Acquisitions
RTD	Real-Time Dispatch
RMS	Recipe Management System
SDT	Single Die Traceability
SPC	Statistical Process Control
WLT	Wafer-Level Traceability
YMS	Yield Management System

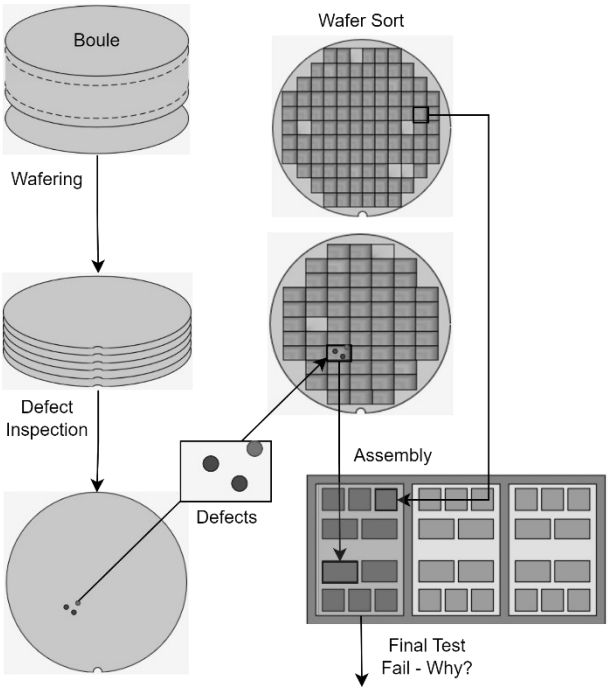

Fig. 6. Using Single Device Traceability for Root Cause Analysis of a Final Test Fail

REFERENCES

[1] J. Holt and A. Weber, "Smart Manufacturing System Engineering for Semiconductor Factories", Invited Tutorial (2024), APC/M Europe.

[2] T. Kimoto, J. Cooper, "Fundamentals of Silicon Carbide Technology", IEEE Press 2014

[3] V. Veliadis, "SiC chip cost, the impact of defects, and the case of price parity with Si", SEMI 2023

[4] TrendForce News, 2024-11-14, Overview of Progress Among 33 Global SiC Manufacturers

[5] End-to-End Smart Manufacturing Report, Porsche Consulting 2024

[6] M. Ono, et al, "Accuracy of Yield Impact Calculation Based on Kill Ratio", IEEE ASMC 2002

[7] D. Baierhofer et. al., Correlation of Extended Defects with Electrical Yield of SiC MOSFET Devices, ICSCRM 2022.

[8] S. Kochoska, et. al., Pulsed Forward Bias Body Diode Stress of 1700 V SiC Mosfets with Individual Mapping of Basal Plane Dislocations, ICSCRM 2022.

[9] S. Zamek, "Analytics Solutions for Compound Semiconductors", Semicon West 2024.

[10] D. Huntley, "Device Traceability and SEMI's Single Device Tracking Initiatives", SEMI 2018.

[11] SEMI E142-00-0125, Specification for Substrate Mapping, January 2025