



## End-to-End Yield Management for Compound Semi

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May 2025

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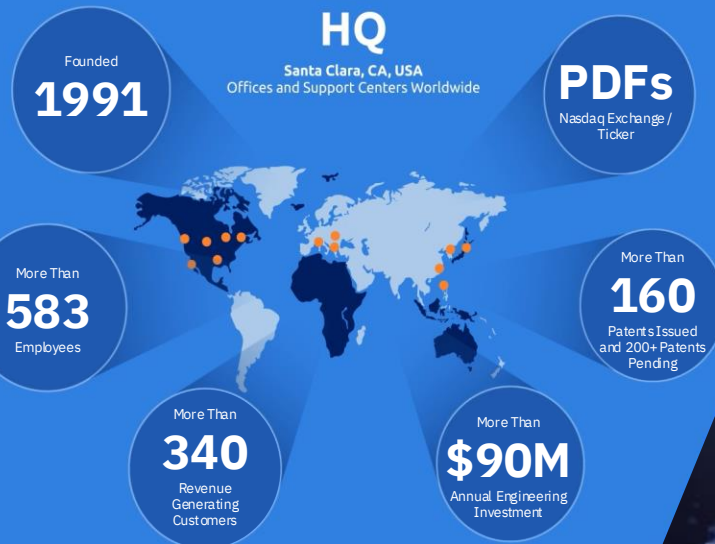
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# PDF Solutions: Leading the Digital Transformation of Semiconductor Manufacturing

PDF Solutions: End-to-End Data Connectivity, Control and Analytics for Systems and Semiconductor Companies



Leading provider of comprehensive analytics solutions for semiconductor manufacturing

We collect and create data from across the supply chain. Then we use AI to enable deeper insights and rapid improvements in yield, quality and operational efficiency.



IC Design



Fab



Sort



Assembly



Final Test



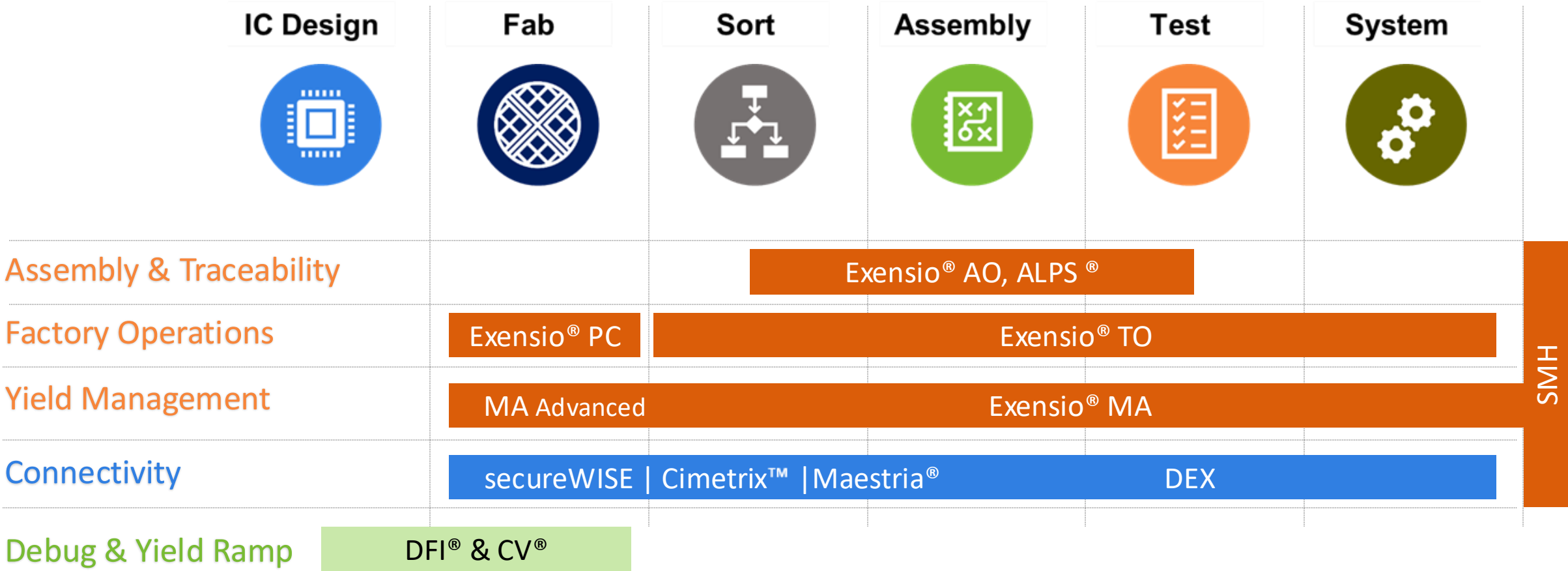
System



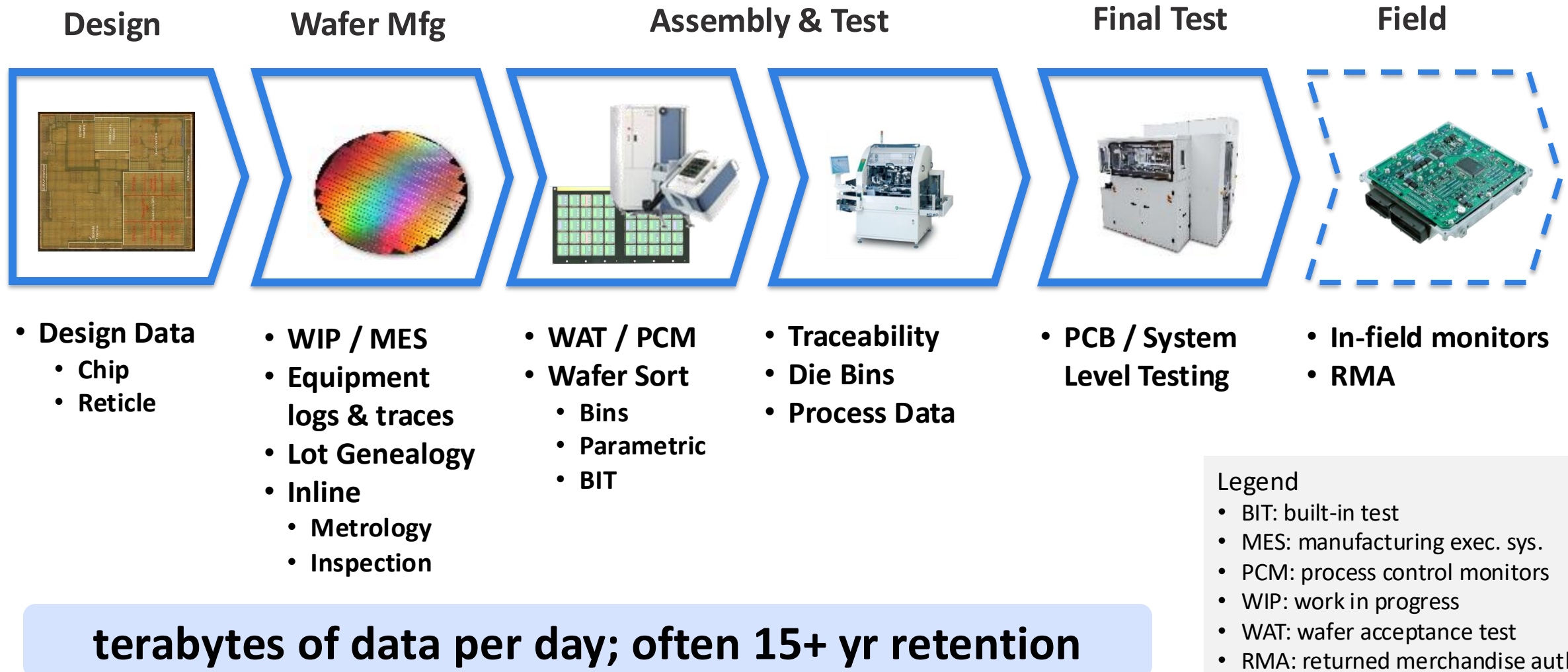
Enterprise

# PDF Solutions overview

For more details:  
[www.pdf.com](http://www.pdf.com)



# Data Collected in Semiconductor Manufacturing



# Customer Base in Compound Semi

Select DM's with a focus on compound semi		Fab Technology			
Customer	Description*	Si	SiC	GaAs	GaN
A	In top 10 in Power IC's & modules	✓	✓		
B	In top 10 suppliers of RFIC	✓		✓	
C	In top 10 suppliers of RFIC	✓		✓	✓
D	In top 5 suppliers of LED's	✓	✓	✓	✓
E	In top 10 in Power IC's & modules	✓	✓		
F	In top 10 in Power IC's & modules	✓	✓		✓
G	In top 3 GaN DM				✓
H	In top 10 in Power IC's & modules	✓	✓		
I	In top 10 in ADAS and IoT	✓	✓		✓
J	In top pure-play foundry for SiC	✓	✓		
K	Niche power IC	✓	fabless		

## Notable customers as of 2024-E

Other technologies, (e.g. InP) omitted due to the low wafer volume

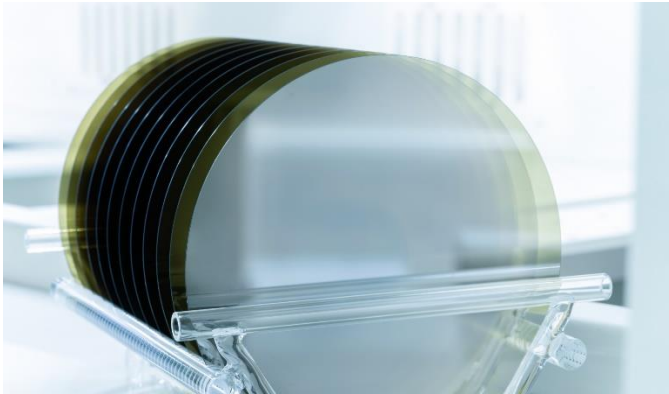
Big Data Analytics  
is deployed in  
**12 large manufacturers**  
IDM / Fabless / Foundry  
+ Material Suppliers



# Example of SiC Manufacturing

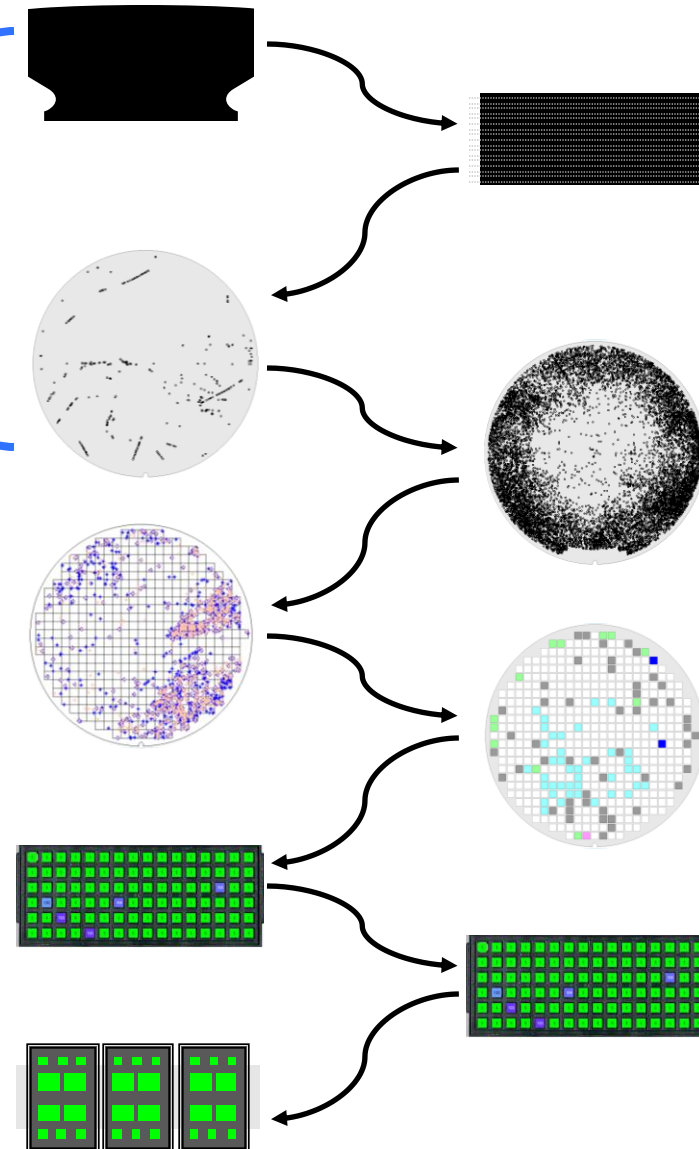


source: CompoundSemiconductors.net, 2017



source: SICC, 2024

>30%  
of the final  
product cost



Boule Growth

Cutting

Grind / Polish

Epitaxy

Wafer Frontend

Backside Process

Wafer Burn-In

Electrical Sort

Assembly

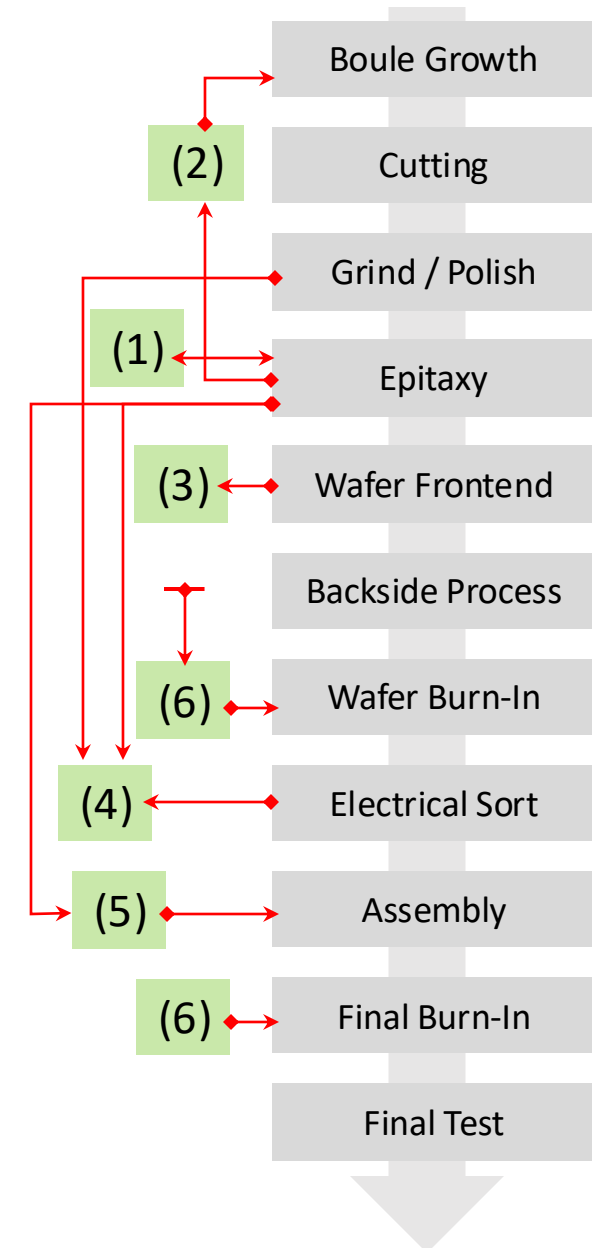
Final Burn-In

Final Test

# Examples of End-to-End Analytics

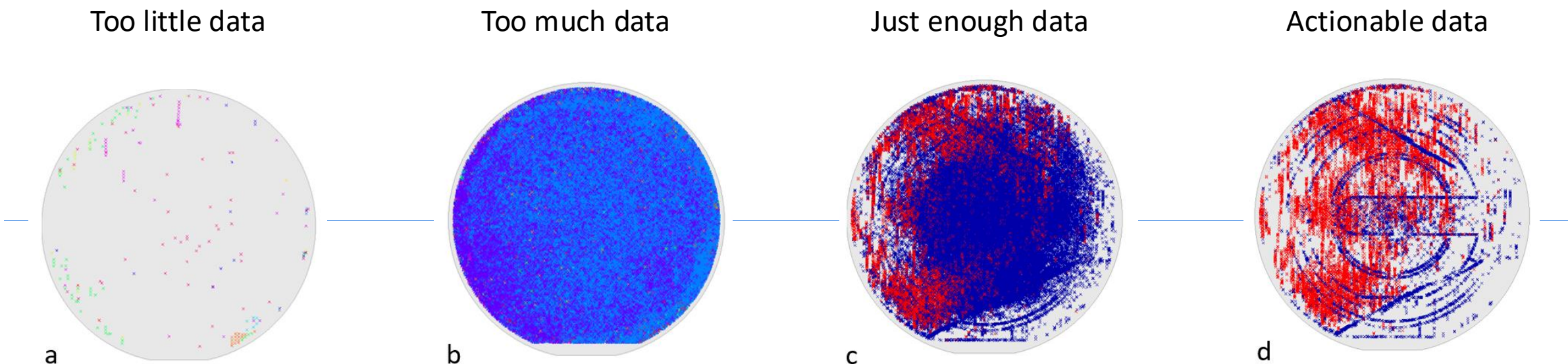
#	Use Case
1	Defect stacking and re-binning for root-cause analysis
2	Reconstructing boule defectivity from epitaxial defects
3	Etch process parameters to metrology correlation
4	Substrate defect yield impact & Defect Kill ratio analysis
5	Die screening and ink-out maps for automotive
6	Predictive Burn-In based on PCM and Probe data

Applying production-proven tools for Compound Semiconductors





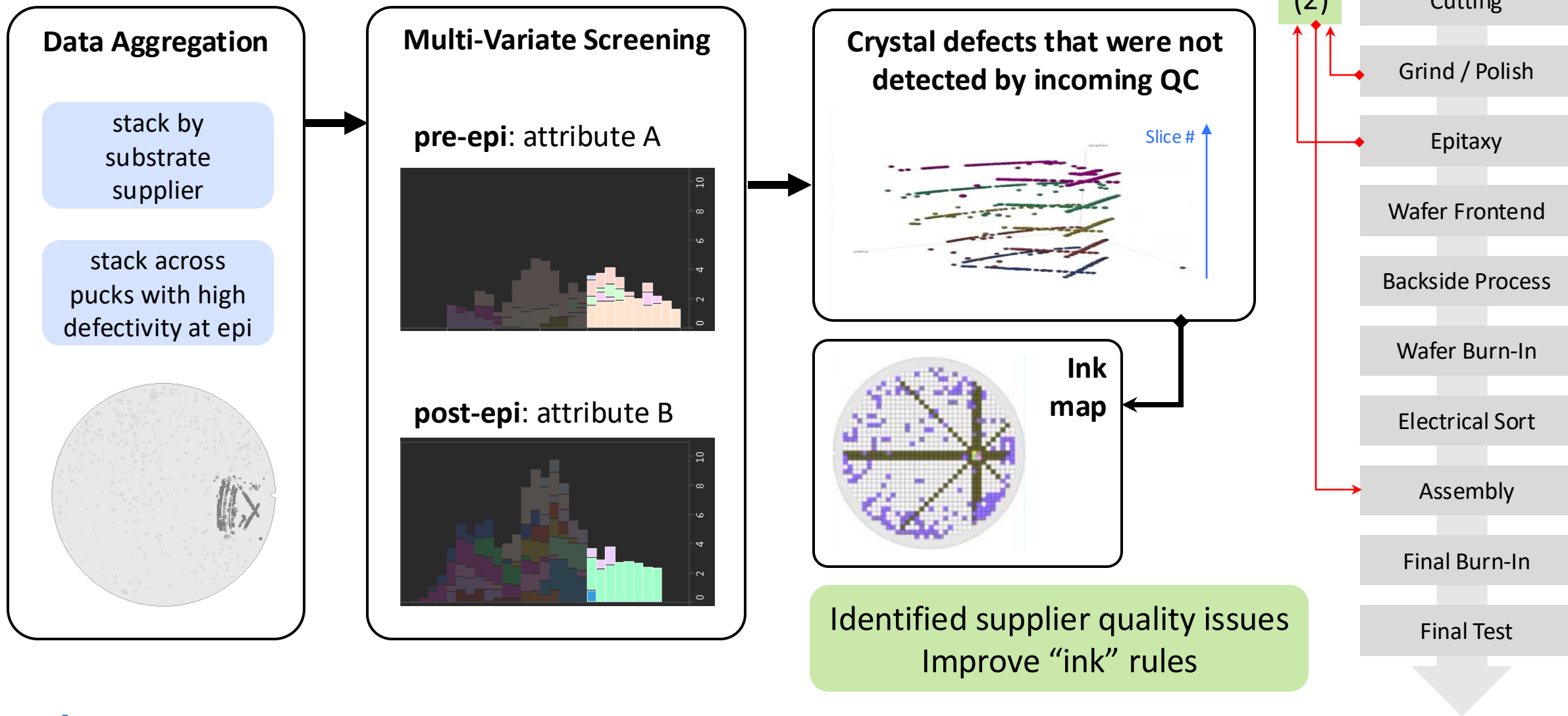
# 1. Defect Management for Root-Cause Analysis



#	stacking by	filtering by
a	---	---
b	+epi product	---
c	+substrate supplier	+defect type
d	+epi reactor	+defect size

Identified epi process issues  
that are substrate-dependent

# 2. Puck defectivity from epitaxial defects



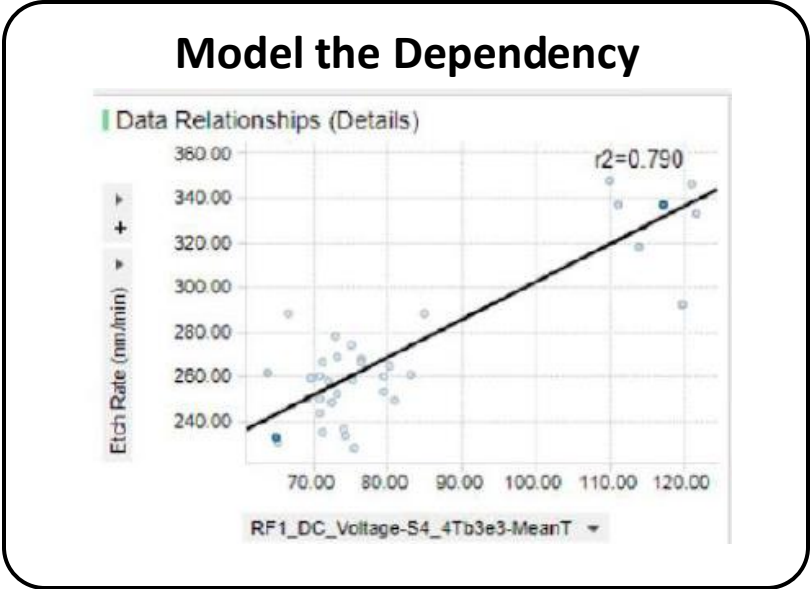
# 3. Etch Parameters to Metrology Correlation

Problem: InP etch exhibits high excursions in etch rate

Univariate Corr. Screening

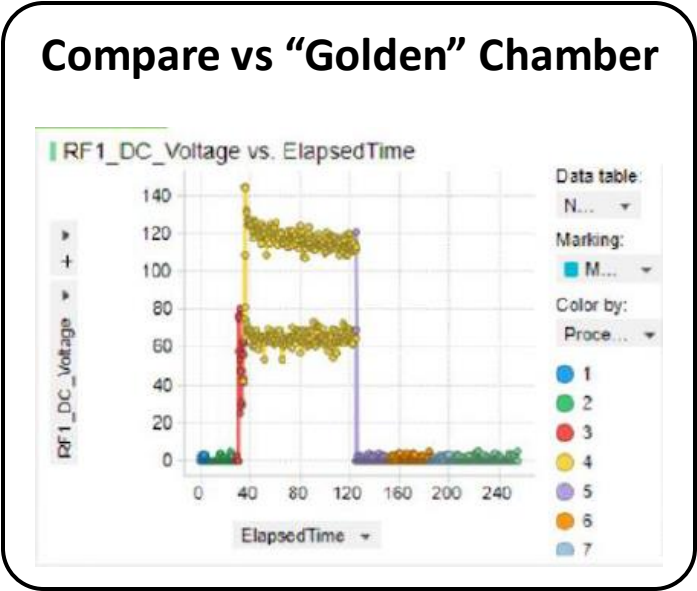
Data Relationships (Linear Regression)

Y (numerical)	X (numerical)	p
Etch Rate (nm/min)	RF1_DC_Voltage-S4_4Tb3e3-MeanT	1.5
Etch Rate (nm/min)	RF1_DC_Voltage-S4_4Tb3e3-Area	1.8
Etch Rate (nm/min)	RF1_DC_Voltage-S4_4-Max	5.7
Etch Rate (nm/min)	RF2_Reflected_Power-S4_4-Area	1.4
Etch Rate (nm/min)	RF2_Reflected_Power-S4_4-MeanT	1.8
Etch Rate (nm/min)	RF1_DC_Voltage-S4_4-Min	1.3
Etch Rate (nm/min)	RF1_Reflected_Power-S3_3-Max	2.7
Etch Rate (nm/min)	RF2_Forward_Power-S4_4Tb3e3-M...	7.5
Etch Rate (nm/min)	Foreline_Pressure-S3_4-Max	1.5
Etch Rate (nm/min)	RF1_Reflected_Power-S4_4-Max	3.9
Etch Rate (nm/min)	Helium_Flow-S2_2-Max	8.2
Etch Rate (nm/min)	RF1_DC_Voltage-S4_4Tb3e3-StdDe...	1.1
Etch Rate (nm/min)	RF1_Reflected_Power-S4_4-Area	2.5





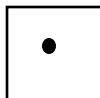
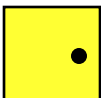
Automated root-cause analysis

- Equipment traces are extracted as indicators
- Indicators correlated to process outcomes
- Excursions in outcomes are tied to the excursions in equipment trace data



## 4. Defect Yield Impact & Defect Kill ratio analysis

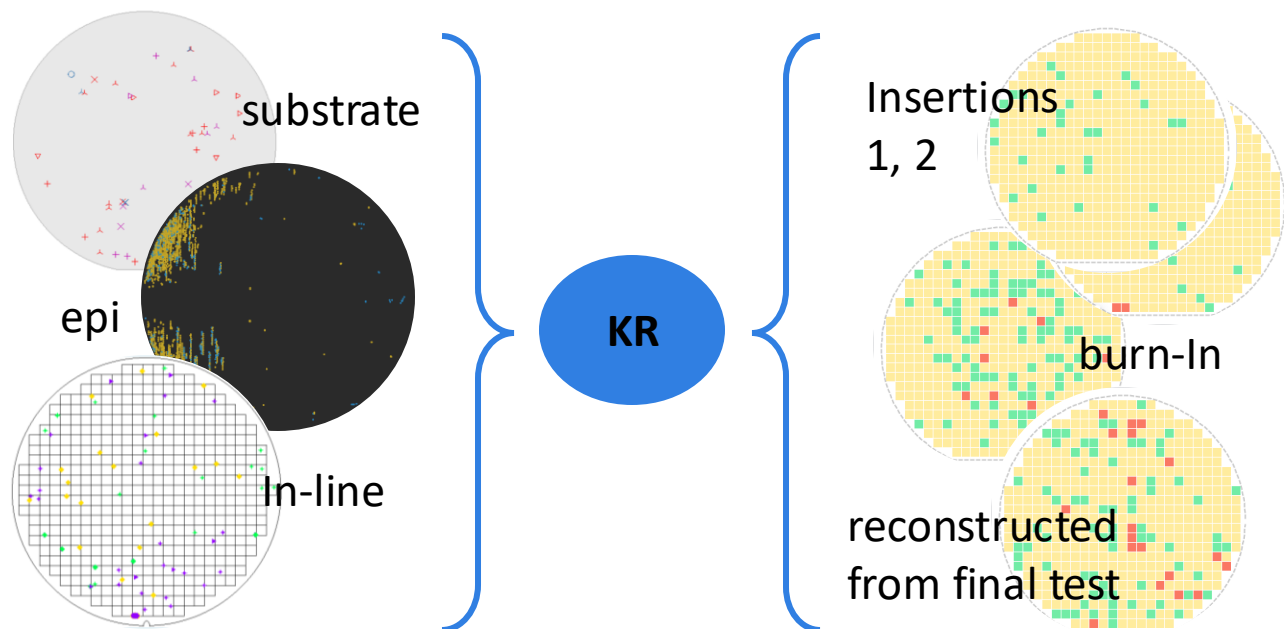
### In the Silicon World

	PASS	FAIL
CLEAN	a 	b 
DIRTY	c 	d 

$$\begin{aligned} \text{KR} &= 1 - \frac{Y_D}{Y_C} \\ &= 1 - \frac{c}{a} \cdot \frac{a+b}{c+d} \end{aligned}$$



### In Compound Semi

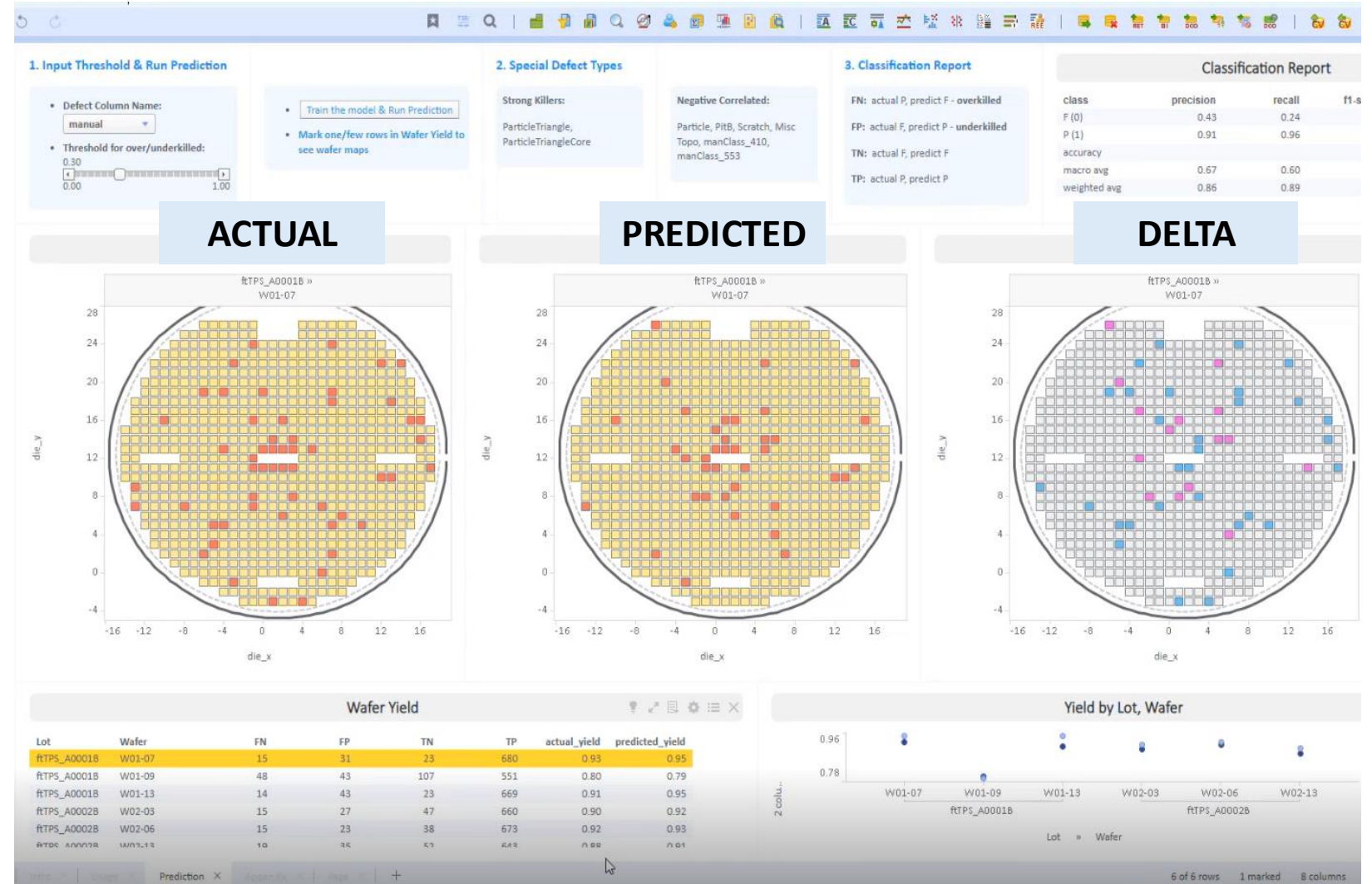


Complexity / Defectivity / Data Volume / Traceability  
→ better models are needed



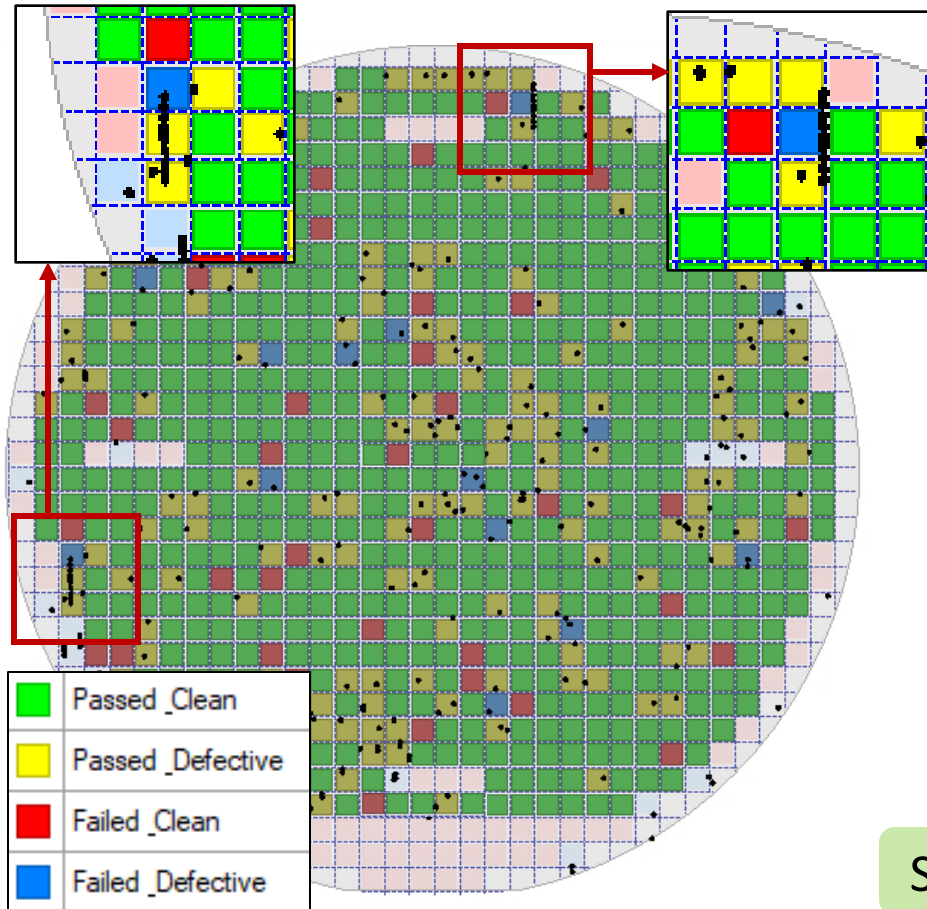
# 4. Defect Yield Impact & Defect Kill ratio analysis

- Using defect maps to predict die state (pass/fail)
- Used for:
  - SiC epi substrate grading
  - Epi supplier benchmarking
  - Substrate-product assignment

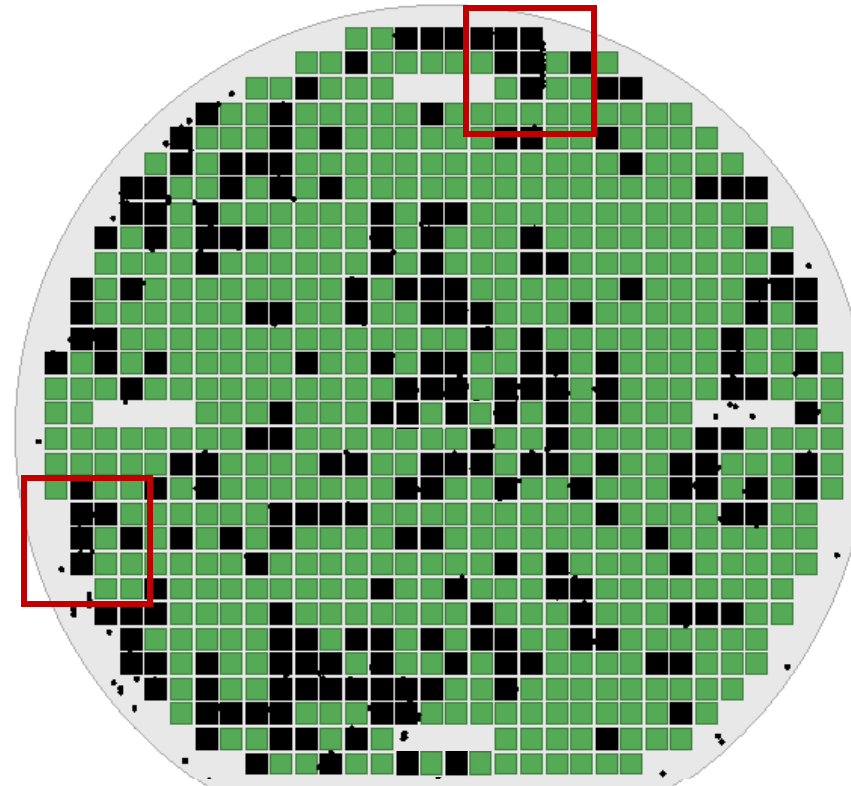


# 5. Die screening and ink-out maps for automotive

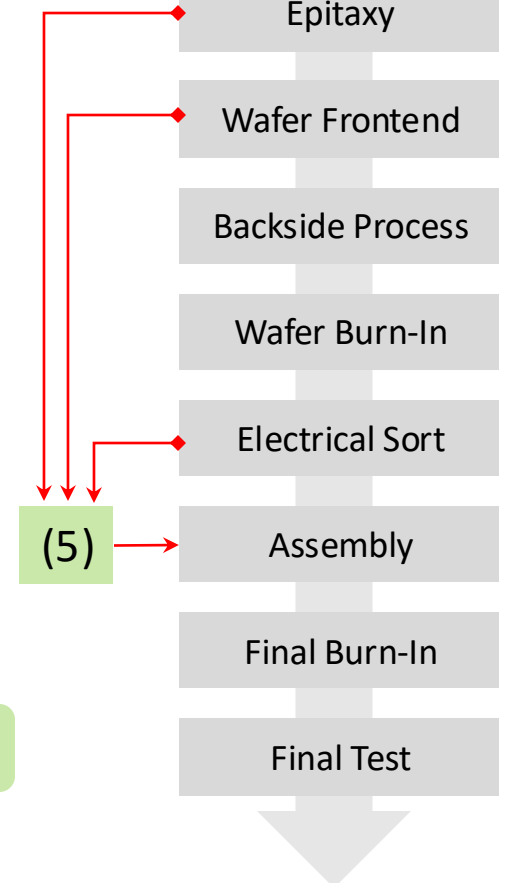
Probe-Defect Map



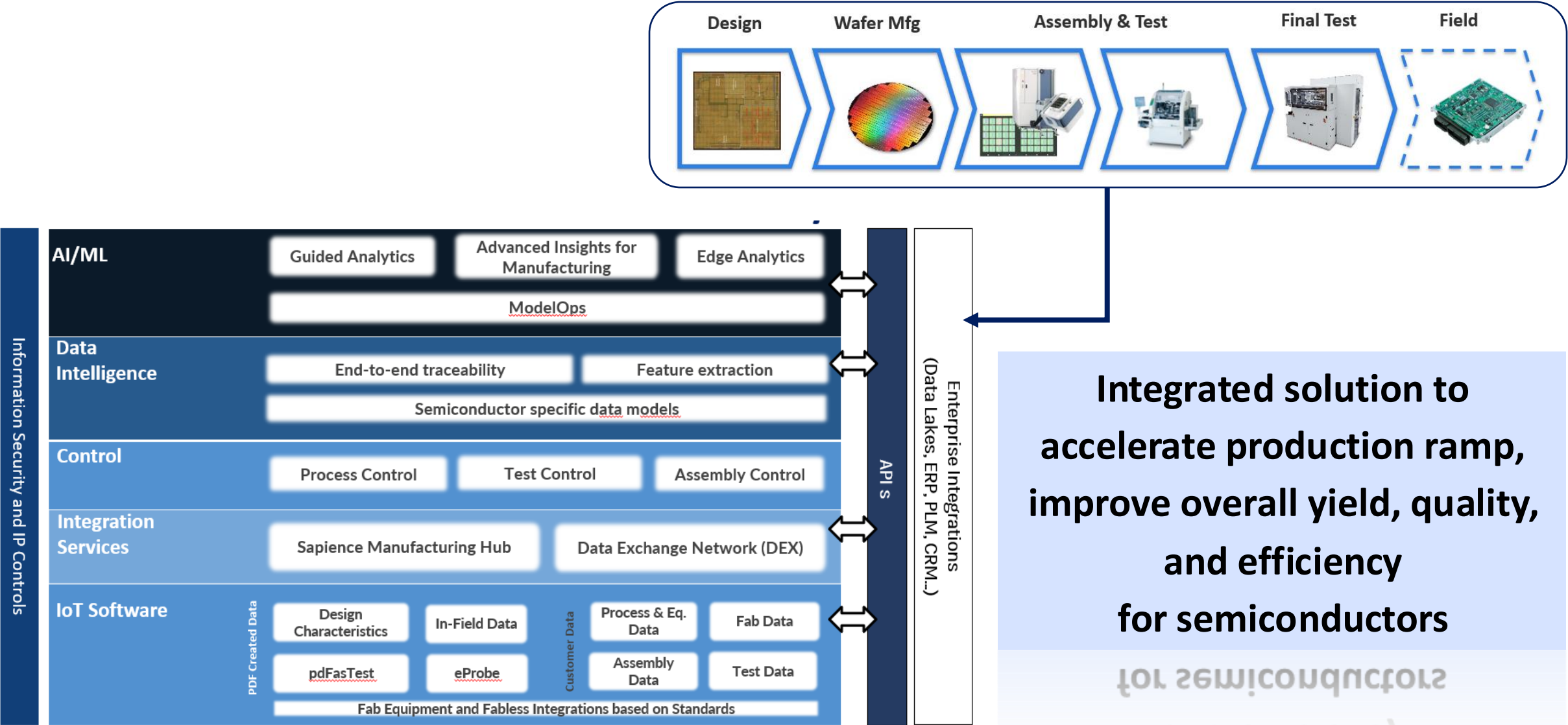
Ink-out map for assembly



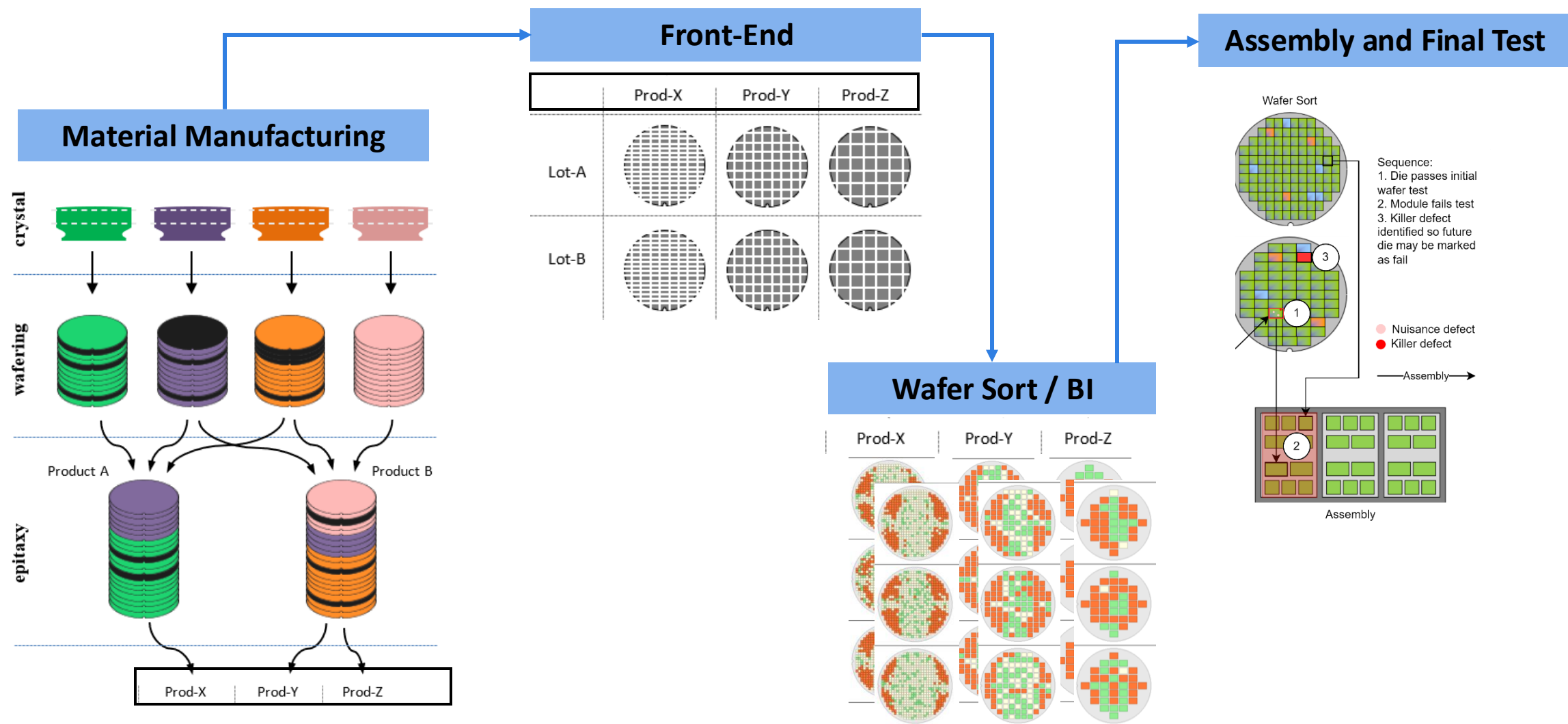
Screen-out defective die for yield and quality



# Under the Hood: Big Data Platform

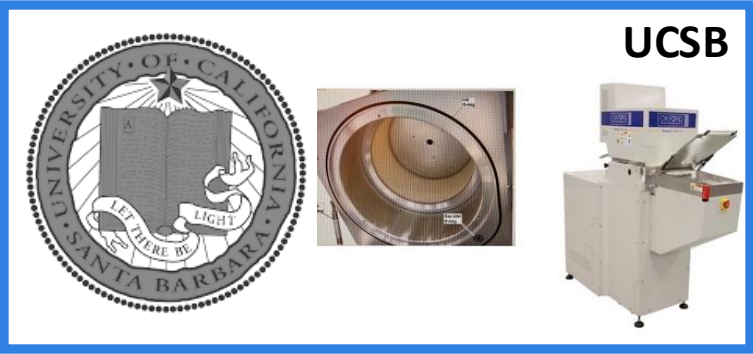


# Under the Hood: Full Traceability





# Supporting ME Commons & CA DREAMS



UCSB



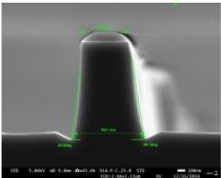
USC

Two Chambers:  
Different Physical Geometry

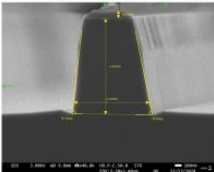


Perform InP etch  
DOEs on Both and  
measure outputs

Etched at UCSB  
Etch Rate ~260 nm/min



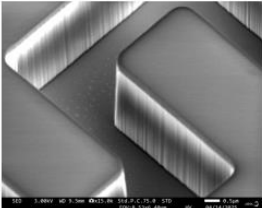
Etched at USC  
Etch Rate ~290 nm/min



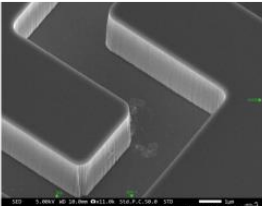
Use PDFS Exensio software  
to match chambers using  
DOE results.

Choose GaAs UCSB Recipe  
Apply matching from DOE  
Etch at USC - Compare

USC  
Etch Rate 1030nm/min  
Mask Select: ~41



UCSB  
Etch rate 1000nm/min  
Mask select: ~38



Single Sample  
Recipe Transfer  
Achieved



**DREAMS**  
Defense Ready Electronics  
and Microdevices Superhub



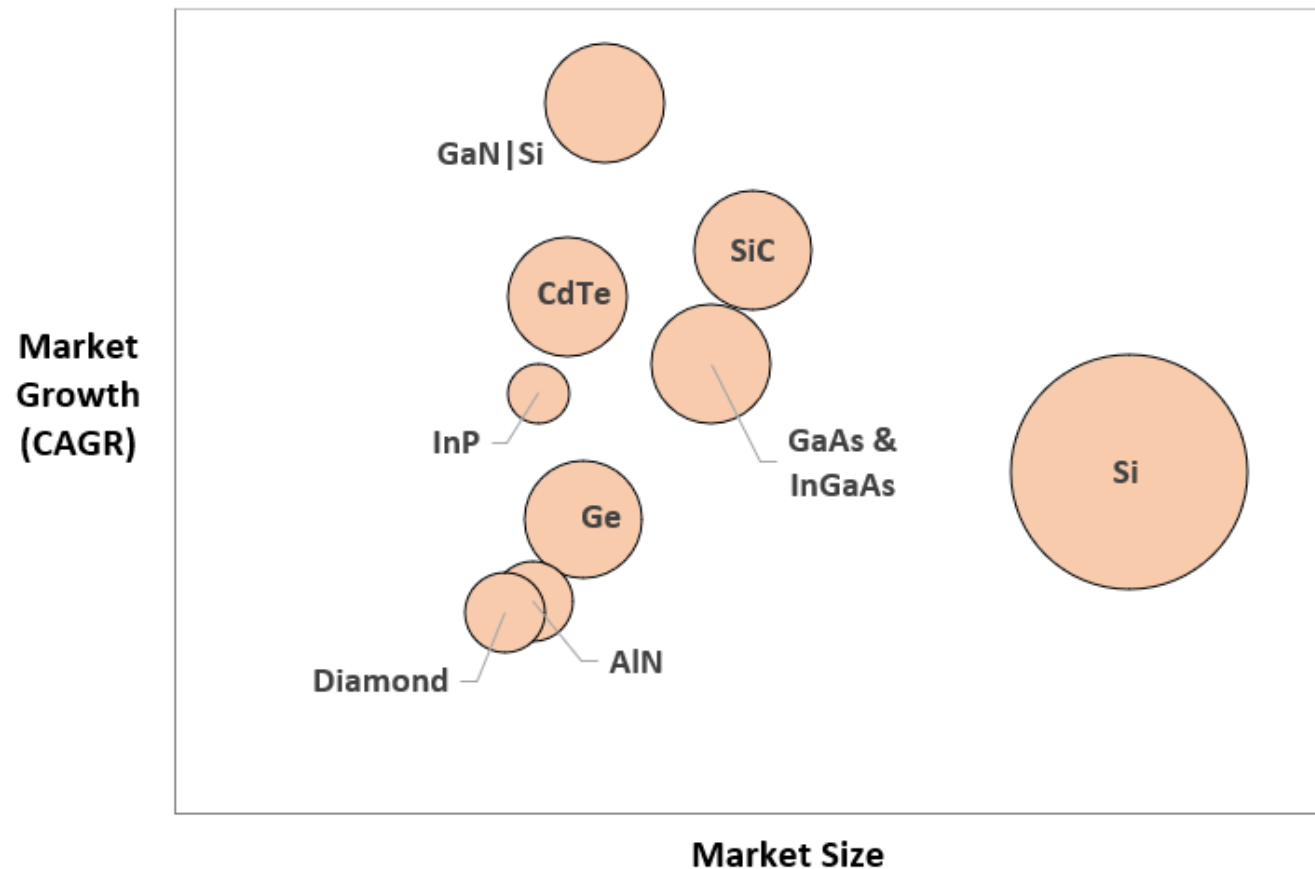
Demonstration of a one-shot process transfer between etch tools

# Final Notes

- Compound Semi industry is decades behind CMOS in maturity
- But progress can be accelerated using data analytics



Take your  
next step



# Thank You

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