PDF/SOLUTIONS° 2025 Users Conference

Deep Dive PDF Solutions Technical Strategy

Peter Kostka

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Deep Dive PDF/SOLUTIONS® SIEMENS

Rishi Bamb

SOLUTIONS®

Scan Fails

Understanding what are Scan Fails

Definition:

Scan fails occur when a chip fails during scan testing, which is used to verify digital logic and detect manufacturing defects.

Why they happen?

- Defective logic gates or interconnect
- Timing issues or stuck-at faults

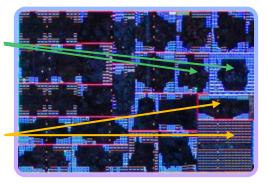
How can they help to improve Yield?

Scan Testing at Wafer Sort

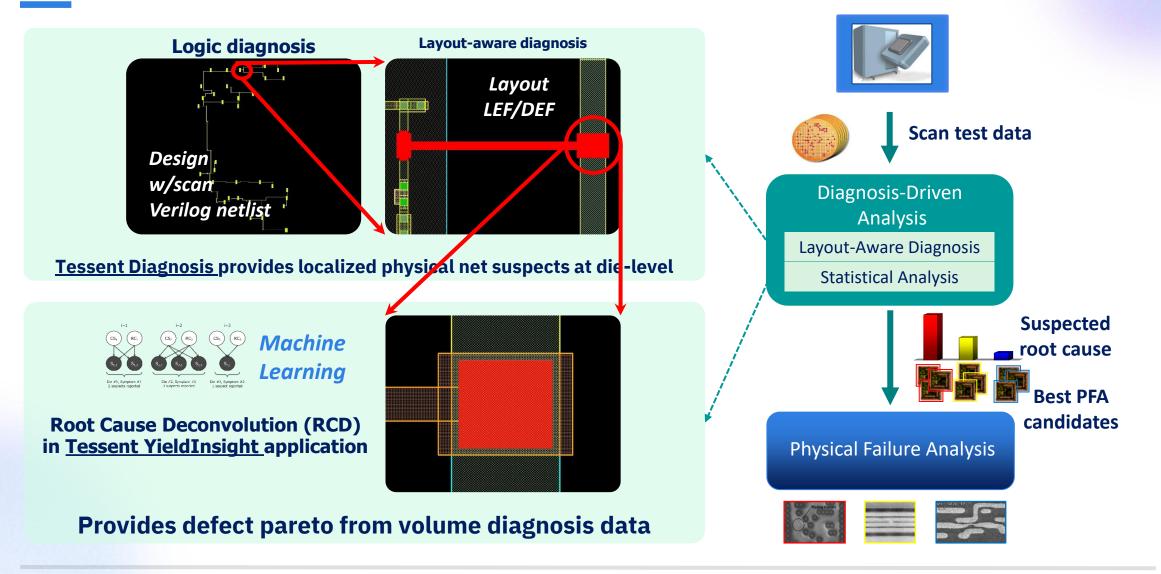
order	bin	passfail	bin_description
1	9	F	Pin Shorts
2	8	F	Pin Opens
3	39	F	jtag
4	17	F	IDDQ
5	11	F	scan_logic
6	5	F	scan_stuck
7	16	F	scan_delay
8	12	F	mbist
9	19	F	DDR
10	25	F	HSIO
11	1	Р	functional

GPU Logic

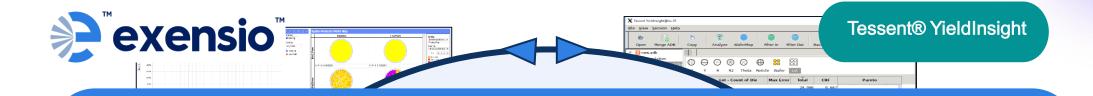
GPU SRAM



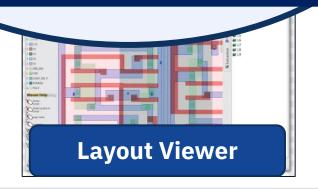
Tessent Diagnosis and Tessent YieldInsight



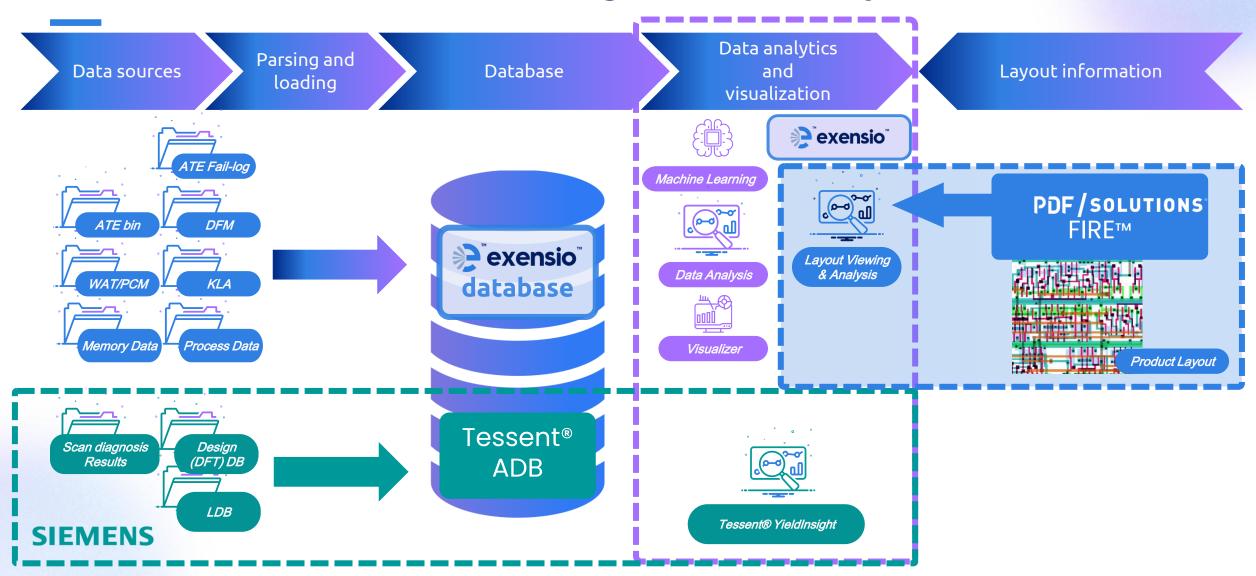
Typical Approach and Challenges



Needs efficient single-UI one-stop solution to product failure analysis including scan test and layout!



Exensio MA with Tessent® Scan Diagnosis Data & Layout Review



Why Choose Exensio's Unified Platform?

Tessent Yield Insight + Exensio MA + Layout Review

- Evolve from NPI stage to HVM-ready solution
- Enrich yield analytics with scan diagnosis and layout design information
- Enable Product engineers with fast, secure access to critical layout information
- Enables flexible, scalable hybrid deployment across cloud and on-premises environments

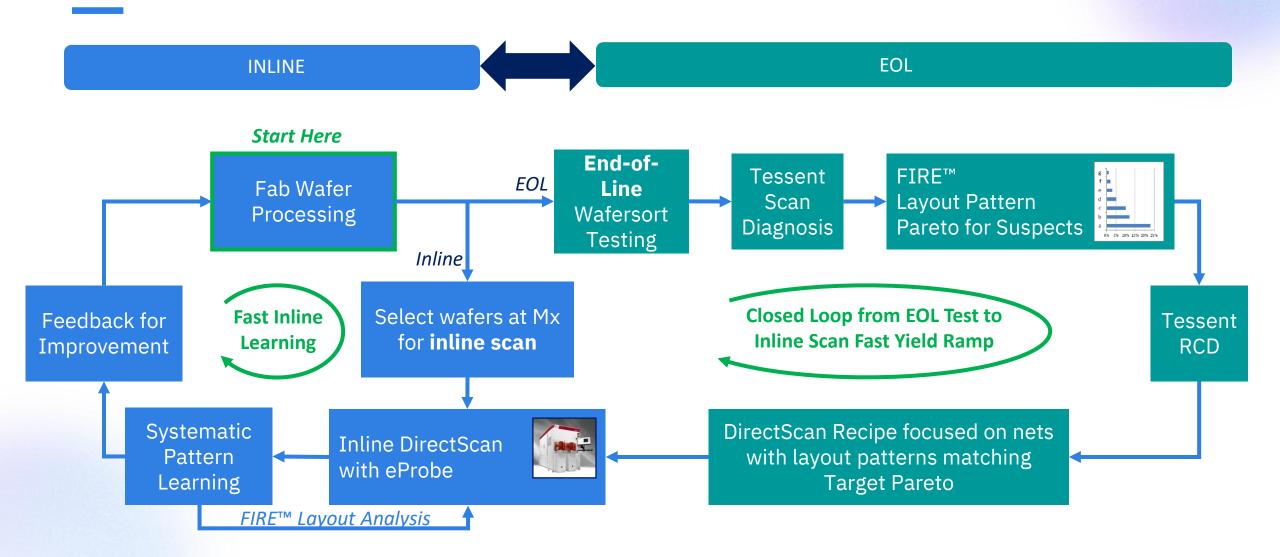
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Demo



Application: Optimized eProbe DirectScan using Tessent® diagnosis results



Key Takeaways

Exensio AIM Scan Analytics with Layout Review

- Transform scan diagnostics from an NPI-focused tool into an HVMready solution
- Increase probability of *pinpointing* exact fail location in layout
- Make scan diagnosis and layout information accessible to a broader group of engineers
- Opens many opportunities for new applications

Thank You PDF/SOLUTIONS

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