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## DirectScan : Technology, Application and Adoption

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# eProbe : Designed for Next Gen Semi Scaling

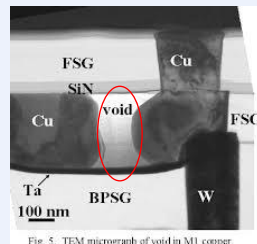
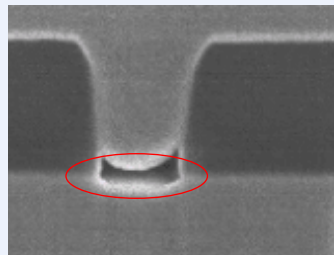
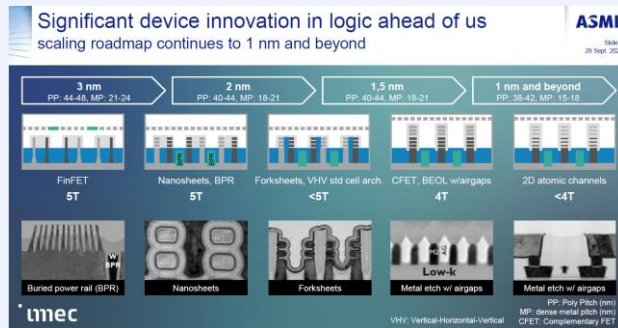


Fig. 5. TEM micrograph of void in M1 copper.



## Key Trends/Drivers

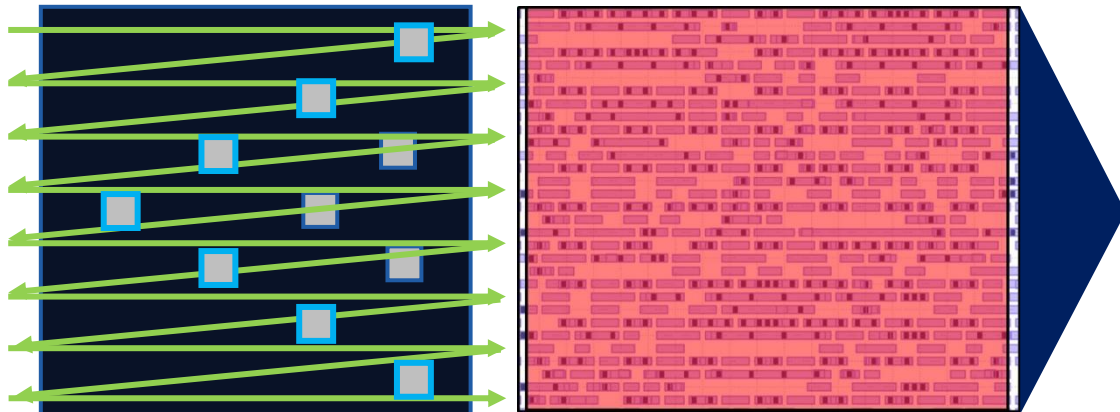
- Increasing 3D nature of process integration today
  - Complex FEOL (Finfets, GAA, nano-ribbons)
  - Multilevel MOL stacks with multiple colors
- Drives more buried defects that are optically unresolvable. Needs electrical resolution possible with eBeam Voltage Contrast (VC) Inspection
- Most defects are not random but increasingly systematic. Driven by pattern/layout weaknesses, spatial trends and product specificity

## DirectScan = eProbe(PointScan) + FIRE + Exensio

- eBeam VC Inspection Solution designed ground up towards this
- VC Detection** : Focus on electrically relevant defects
- Design-aware Inspection** : To understand layout weaknesses
- Product-based Learning** : Yield learning directly on product vehicle

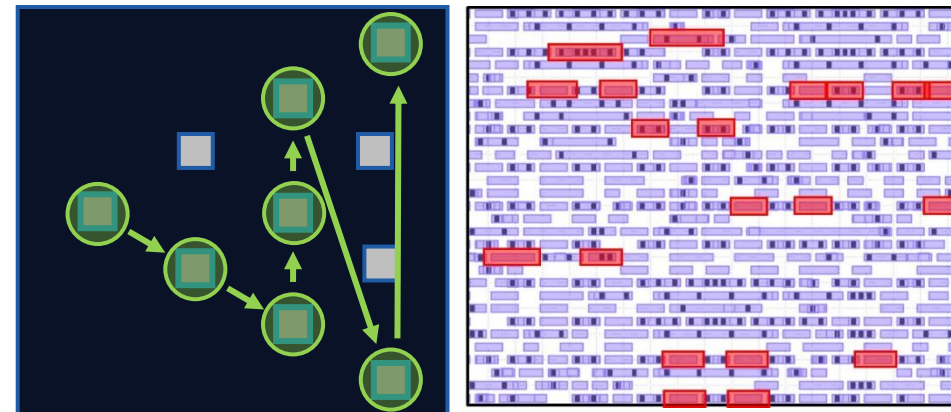
# eBeam Inspection : Conventional vs. eProbe-PointScan

## Conventional ebeam Inspection



- Region of interest scanned 100% by rastering
- Defective Pixels (grouped) reported in KLARF
- No knowledge of metal stubs during scanning
- Post inspection overlay to GDS is possible

## PointScan Inspection



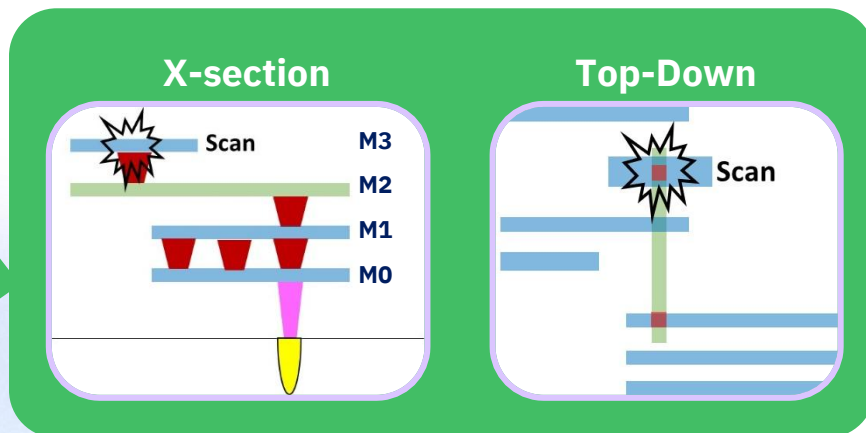
- Only pads of interest are scanned
- Defective PADS aka DUTs reported in KLARF
- Design Aware Inspection : eProbe knows precise pad type and GDS location *while scanning*

Continuous  
Stage Motion

- eProbe-PointScan acts as a contactless ebeam tester
- Scans Billions of DUTs per hour
- 20-100x faster than conventional single beam tools for sparse inspections

# Systematic Defects needs Targeted Inspection

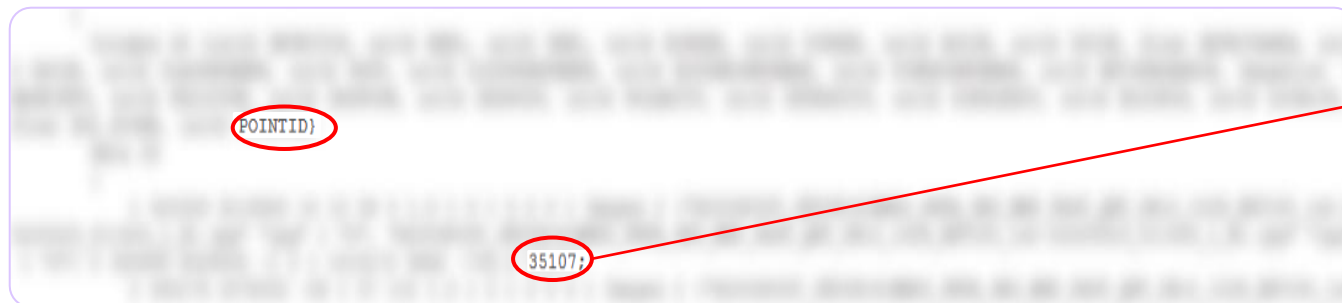
Defect Type	VC Type	Inspection Layer	Location Constraint	Measure. Unit	VC Inspectable Locations / wafer	Total Locations / wafer	Ratio (%)
BEOL : V2	Open	M3 CMP	>Non-redundant V2 >M3 grounded to wafer >Smallest L/W combination	Meters	3.05	120.6	2.53
MOL : Buried Gate-Drain	Short	MOL Contact CMP	>Specific Xtor polarity >Avoid High_Ikage Xtors >Avoid nbh gate-drain contacts	Million DUTs	23.1	2203	1.05
FEOL : Gate Stringers	Short	MOL Contact CMP	> Specific SRAM Array contacts	Million DUTs	493.2	1739	28.36



**VC Inspectable Locations << Total Available Locations**

# DirectScan : Identify Product Weaknesses

## Example eProbe KLARF output

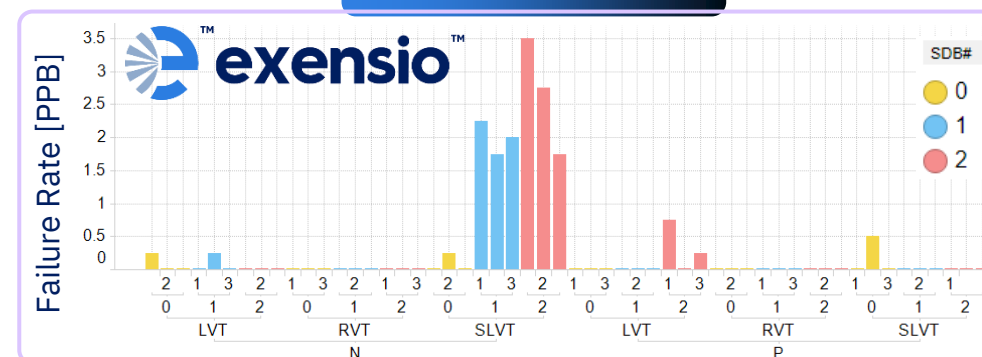


## Attribute Lookup Table

Attrib	CX	NP	VT-flavor	Track	SDB#	COAG
35101	CA	P	LVT	7	1	N
35107	CA	N	RVT	2	0	N
35235	CA	N	RVT	1	2	N
35239	CA	P	LVT	1	0	N
35339	CB	P	SLVT	6	0	N
35400	CB	N	SLVT	5	0	N
35457	CA	N	LVT	1	0	N
35461	CB	P	LVT	6	0	Y

- Attribute info for every inspected DUT pre-mined from FIRE analysis
- Attributed info for every defect is reported
- Fail Rates easily calculated for any attribute
- Design/layout weaknesses easily identified**

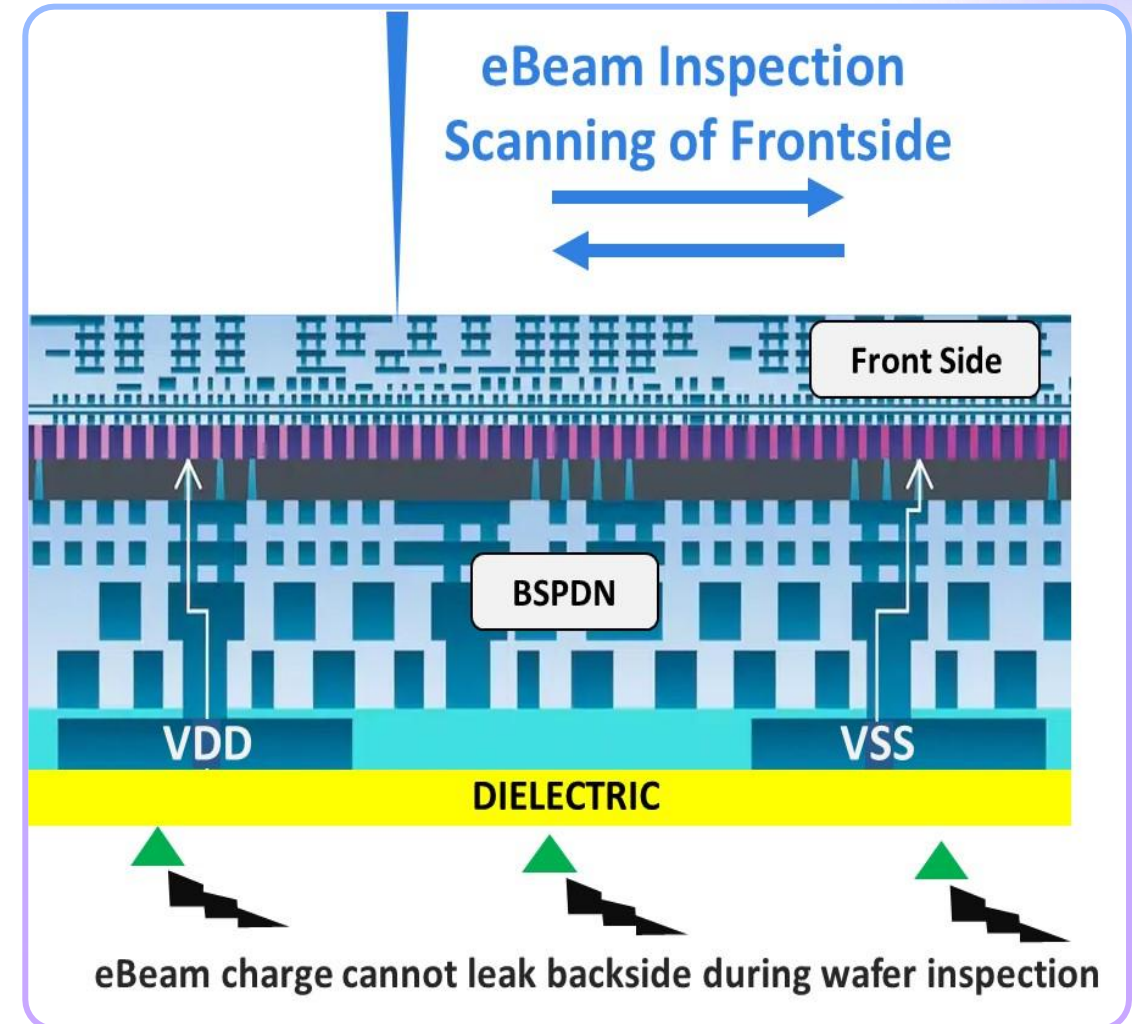
## MOL Fail Rates



← Transistor SubTypes →

# PointScan for BSPDN & 3D-DRAM Wafer Inspection

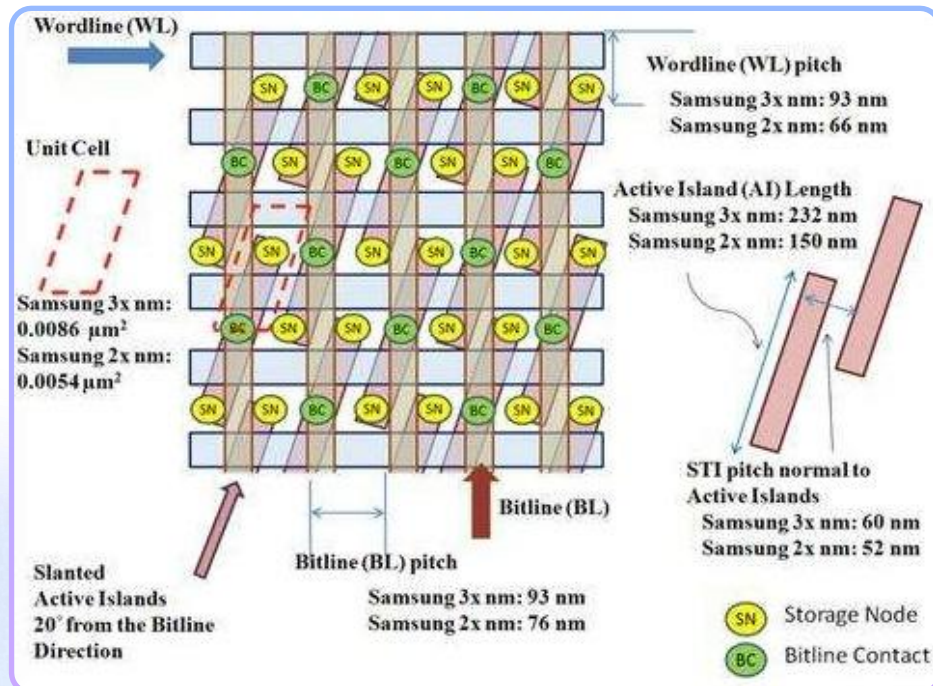
- **BSPDN wafer scan:** No clear path for ebeam charge leakage to backside
- **Strong charging, defocus, beam shift** during eBeam inspection. Not easily amenable to ebeam inspection
- PointScan is favorable due to **lower charge accumulation**
- Demonstrated scan on BSPDN wafer in **advanced Logic**



# PointScan : Allows Controlled “Charge and Sense”

- Successful detection of **Storage Node Shorts in DRAM array**
- Controlled “Charge and Sense”** is Unique to PointScan
- Inspection Methodology: **Charge WL & immediately Sense Array**

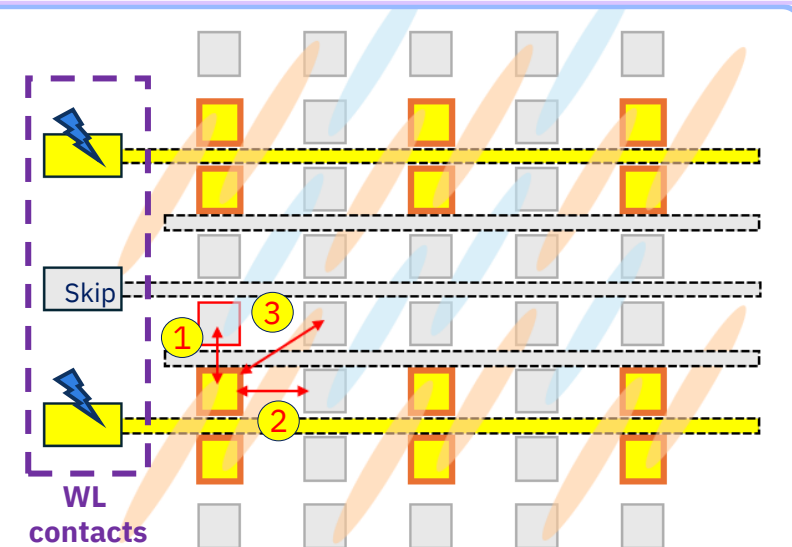
<https://www.eetimes.com/samsung-2x-nm-lpddr3-dram-scales-memory-wall/2/>



- Island-to-island short detection from Surface or embedded defects
- Charging alternate WL contacts excite certain island nodes
- Can be used to detect shorts to floating island nodes

- Charge alternate WL
- Only Feasible by eProbe Point Scan

**Turn Bright**



# DirectScan Adoption at Leading Edge

- **Leading Edge Logic** : Dominated by (A) MOL opens/shorts (B) BEOL systematic contact opens
- **Leading Edge DRAM** : Dominated by Periphery use cases requiring Point Vector Scanning

Product	Scan Area	Layer	Fail Type
Leading-edge Logic	<input type="checkbox"/> Random Logic <input type="checkbox"/> SRAM	MOL	GAA Gate-Drain Shorts GAA Gate-Cont Open GAA Gate-Epi/Silicide Open
	<input type="checkbox"/> Random Logic <input type="checkbox"/> SRAM	MOL	
	Random Logic	BEOL (M0, 1x, 2x)	Systematic Contact Open
	Random Logic	BEOL (M0, 1x, 2x)	Systematic Mx Shorts (T2T, S2S)
	Random Logic	MOL	Leakage Estimation
	Random Logic	BSPDN	Contact open/short (power Via, Source/Drain Via) (From local/global stress-relaxation)
Leading-edge DRAM	Periphery BL	MOL	<input type="checkbox"/> Gate-Gate stringer shorts <input type="checkbox"/> Gate-Drain shorts
	Periphery WL	MOL	WL-WL shorts WL opens with Localization
	Array	MOL	Array shorts

# Takeaways

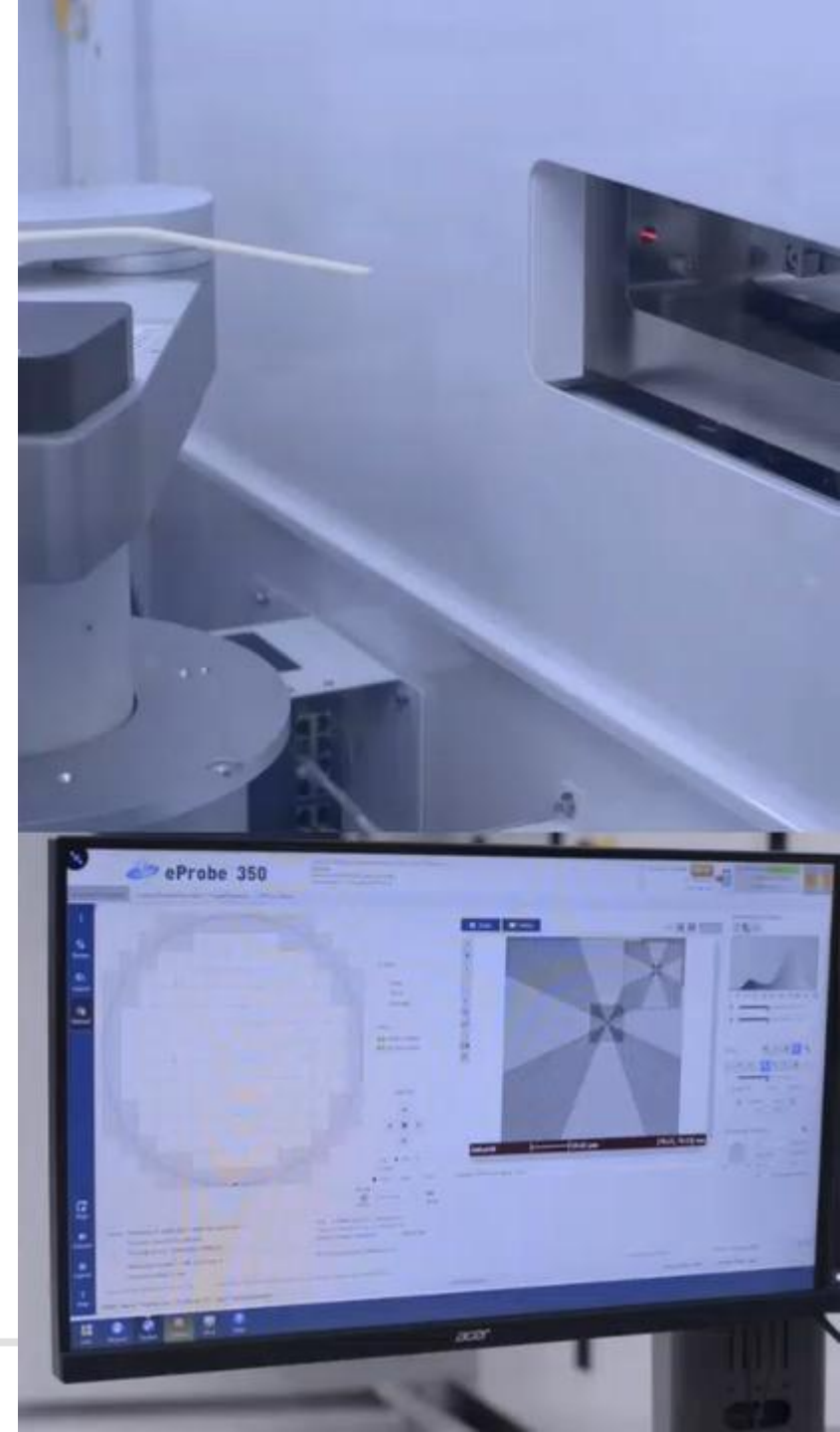
**eProbe** : Designed for Voltage Contrast eBeam Inspection using **PointScan**

**DirectScan** Solution = eProbe(PointScan) + **FIRE** + **Exensio**

- **Pointscan** : High throughput for product inspection
- **Attribute analysis** : Faster TAT in understanding process weaknesses
- **Less Wafer Charging** : Highly suitable for BSPDN and 3D-devices
- **Controlled “Charge and Sense”** : Opens new applications

**2022-2024: Used extensively in leading Logic nodes (FEOL/MOL/BEOL)**

**2024 – 2025: Increasing applications found for DRAM**





**Customer Presentation**



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