03.

A discussion of real-world advanced test methodologies leveraging novel data and AI/ML driven approaches to achieve superior yield, efficiency and device performance.

Panel Discussion With Advantest, Teradyne, PDF Solutions

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Advanced Test
In the Semiconductor Industry

2025 USERS CONFERENCE

Dec 3, 2025

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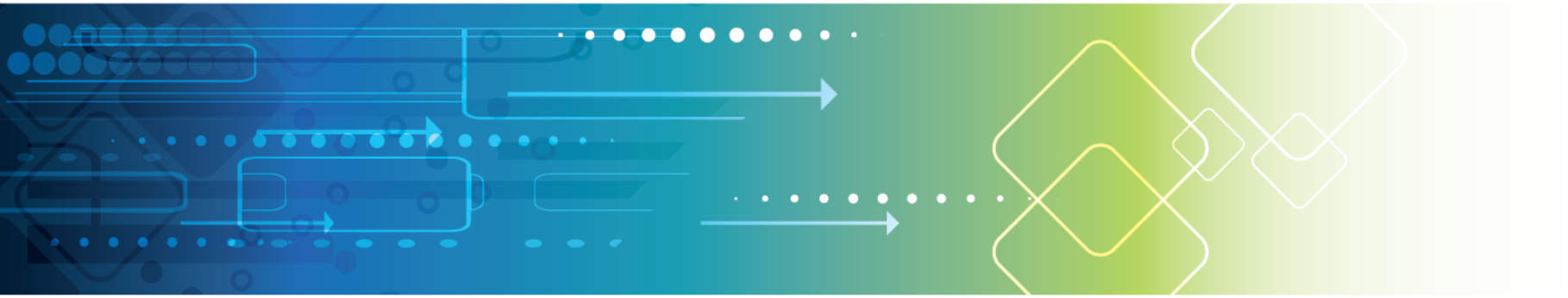
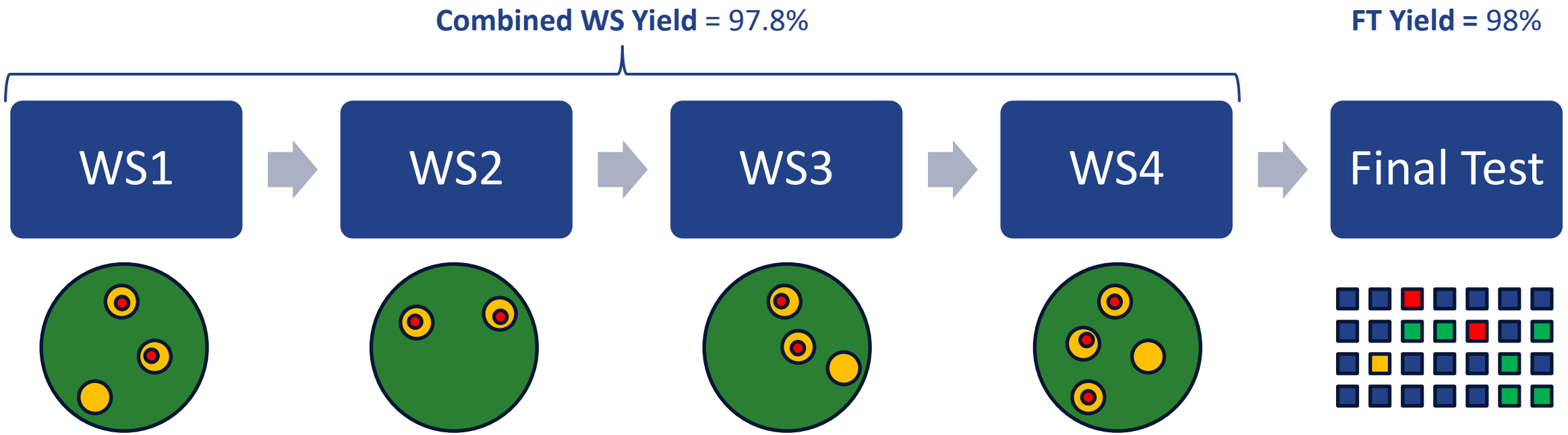
TERADYNE

Enabling Advanced Analytics with Archimedes



FT Fault Predictor



Model Assumptions:

- Identify a failing die in a 100-die area — over kill all 100 die
- Strive for > 90% accuracy
- Overkill 1.6% yield impact
- 1% of Yield Increase at FT

TERADYNE

ADVANTEST

The “Vmin” App

How Machine Learning can help Test Engineers

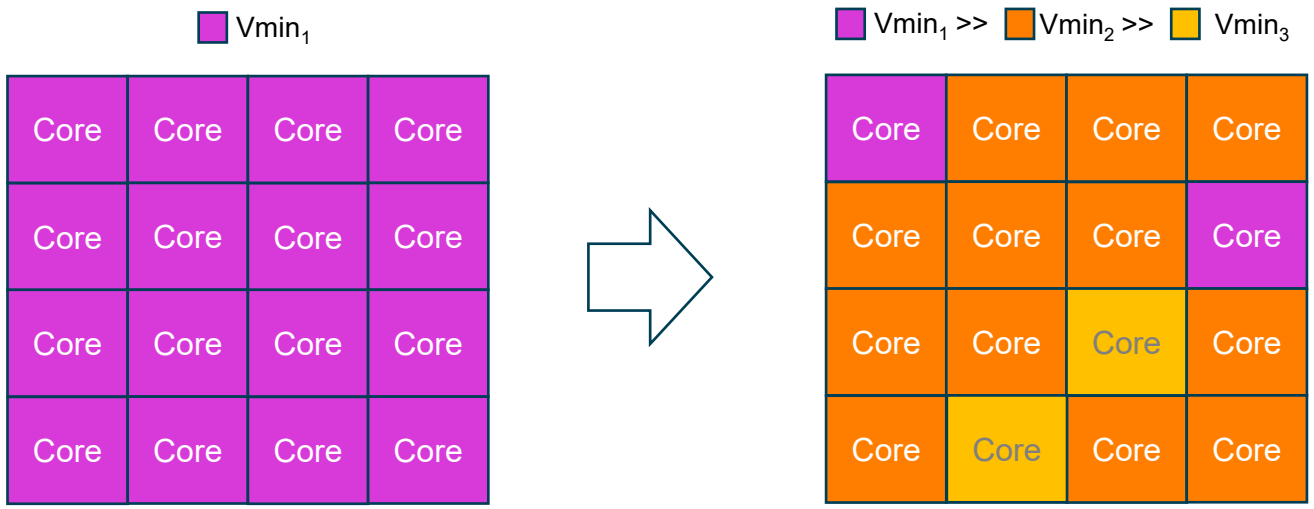
ACS Product Marketing

December 2025

ACS

The Vmin Test

The Vmin test in semiconductors, determines the minimum operating voltage at which a chip or circuit block can function reliably without errors.



Before Vmin Tuning
Power = P_1

After Vmin Tuning
Power = P_2 (<< P_1)

Power Efficiency: lowering operating voltage reduces power, which is vital for mobile, battery-powered devices and also high-performance computing devices.

Voltage Sweeping: the supply voltage is gradually reduced during testing while running functional patterns or stress workloads.

How Machine Learning can help Vmin Test

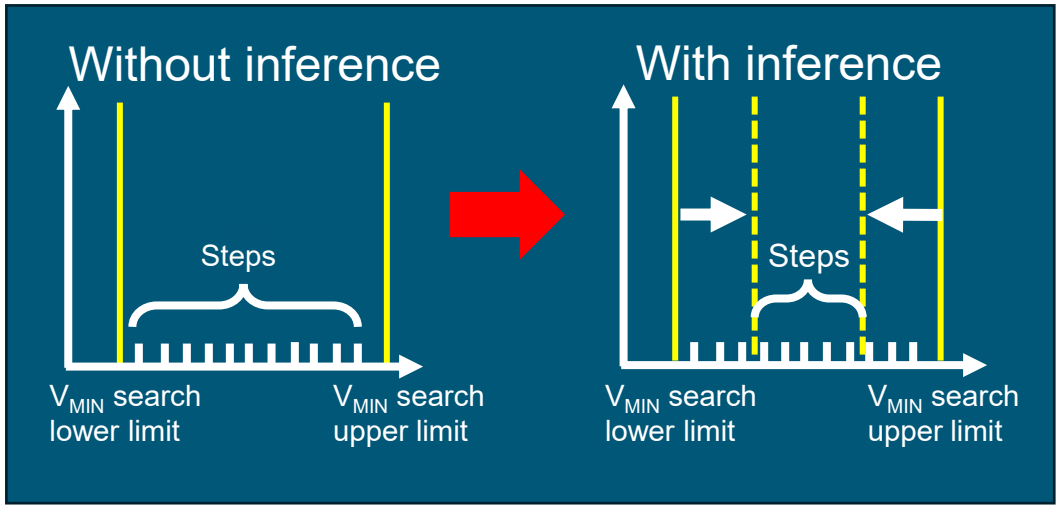
Problem: Extended test duration due to efforts to lower power consumption in multi-core SoCs

Goal: Optimize power per core by tuning Vmin without compromising performance, while accelerating Vmin search to reduce overall test time.

How ML can help: Utilize ML inferencing to predict likely Vmin per-device and narrow the search limits to speed searches.

Results: reduce significantly Vmin test time and at the same time reduce the power consumption of the devices

Insertion point: Wafer Sort or Final Test



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