Impact of the Gate and Fin Space Variation on Stress Modulation and FinFET Transistor Performance

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***Abstract* — Device scaling in advanced CMOS nodes is becoming more difficult due to patterning limitations and complex 3-D transistor integration schemes. This also makes the devices more sensitive to patterning variability. The presented study investigates the impact of poly pitch and fin pitch variability on stress-induced performance variation in 7nm FinFET transistors. Variations in critical dimension (CD) during patterning can alter fin width and spacing, leading to changes in device characteristics. We evaluated device sensitivity using a comprehensive set of test structures and performed TCAD simulations to model the effects. The results confirm that both NMOS and PMOS devices are sensitive to poly spacing, NMOS devices exhibit up to a 13% degradation in drive current, whereas PMOS devices show -11% to +7% variation in drive current, and inter-fin spacing. The dominant mechanism behind these effects is stress modulation, particularly due to changes in the volume and shape of epitaxially grown source/drain regions. These findings highlight the critical role of mechanical stress in FinFET performance and underscore the importance of pitch control to minimize variability and optimize device parametric targets.**

Keywords— FinFET, 7nm technology, TCAD, Poly pitch, Fin pitch, Mechanical stress, Transistor performance

I. INTRODUCTION

Although traditional semiconductor device scaling is slowing down, dimensional reduction remains essential when transitioning to new advanced technology nodes. Scaling entails not only shrinking the physical dimensions of device components but also reducing the spacing between them. This evolution introduces critical challenges, particularly concerning the behavior of mechanical stress within the device structures. A key consideration is whether stress scales proportionally with geometry and how such changes influence device performance, especially in the context of patterning.

In FinFET technology, scaling involves modifications to both fin height and fin pitch (defined as the sum of fin width and inter-fin spacing), as well as gate length and poly pitch. Variations in critical dimension (CD) during the patterning process can lead to changes in width and spacing. With spacer-assisted patterning – currently the dominant technique – fin width and gate length exhibit significantly lower variability compared to their corresponding spacing.

Modern FinFET devices employ multiple performance boosters, among them the "stressors" – architectural elements which can change the stress in the transistor channel. The most common approach is to use stress-introducing material in Source/Drain regions. In such cases, variations in fin and gate spacing alter the stress distribution in the channel region, which in turn modulates carrier mobility and leads to shifts in drive current [1].

This stress–mobility–performance relationship is particularly pronounced when using materials like SiGe for the S/D regions. Due to its larger lattice constant compared to silicon, SiGe introduces compressive stress when epitaxially grown in place of Si, enhancing hole mobility in p-type devices but also increasing sensitivity to geometric variation.

In this study, we designed a comprehensive set of test structures to electrically characterize the impact of gate and fin pitch variability. While our analysis focuses on stress variation as a primary contributor to performance variability, we acknowledge that other factors - such as fin profile or contact area and resistance - can also influence device behavior. These effects are either minimized by our test methodology or considered to have a much smaller impact.

Consequently, our analysis focuses on understanding the contribution of stress modulated effects to transistor performance sensitivity to pitch scaling. This work is a major expansion of an initial study on fin space impact, presented earlier at the Int. Conf on IC Design and Technology, 2025 [2].

In the course of this paper, we will describe the methodology, starting with explanation of experimental details – test structures and measurements, followed by description of the simulation framework used for transistor stress and performance modeling. The subsequent sections will show combined results – experimental data and simulation – for poly space and fin space dependence, explaining how stress modulation impacts device performance. The final discussion will be dedicated to a special case of the so-called Spacer-Assisted Quadrupole Patterning, an advanced technique applied

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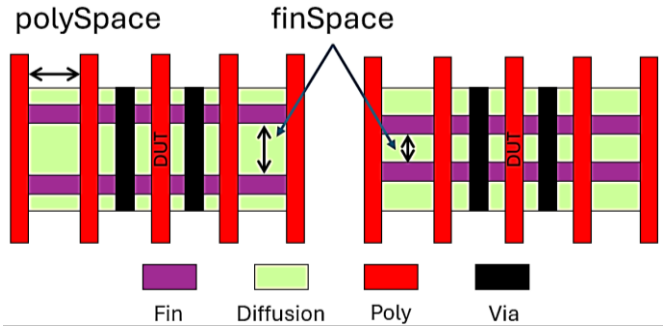

Fig.1 Layout and model parameters of the test structure and the area simulated by the model (dashed), showing Fin, Diffusion, Poly, Trench Contacts and Vias.

to fin patterning, which often leads to interesting pitch walking effects.

While stress–mobility interactions in FinFETs have been widely studied, prior work mainly addressed nominal geometries and global strain techniques. Our study expands previous learnings by quantifying layout-induced variability from poly and fin pitch changes in 7 nm technology.

II. Test Structures and Measurements

The test structures used in this study were designed using design rules for a typical 7nm foundry technology. To quantify the impact of gate and fin patterning on device performance, a special set of dedicated test structures were designed. The layout Design-of-Experiment (DoE) was built for 2-fin and 4-fin NFET and PFET devices, and major DoE factors were: poly pitch, which was systematically varied by up to ±7%, and the fin pitch which was varied by up to ±10%. Each structure was implemented within a controlled layout experiment, enabling the isolation of a single factor of the experiment.

Fig.1 illustrates the layout of the transistors used in this study, highlighting variations in both fin pitch and poly pitch.

The test structures were incorporated into a larger Characterization Vehicle (CV®) test block, developed by PDF Solutions for advanced technology characterization [3]. Each Device Under Test (DUT) was replicated eight times within a compact area to minimize sensitivity to intra-die process gradients and to ensure statistically robust measurements.

Electrical measurements were performed with a parametric tester at room temperature (25 °C), capturing I–V characteristics in both the linear and saturation regimes. Key device parameters, including threshold voltage and drive current, were extracted for each transistor.

To accurately separate intrinsic channel characteristics (mobility) from parasitic components, such as series resistance, a robust de-embedding methodology is required. The measured peak transconductance (gm) is, in fact, strongly dependent on Rext via the relation $gm = gmi / (1 + gmi*Rext)$ [4].

To perform the de-embedding, we applied the Y-Function method described in [5], defined as $Y \equiv Id/\sqrt{gm}$ in linear regime (Vds = 0.05 V). In strong inversion, the linear relationship between Y and Vg enables a robust extraction of the intrinsic threshold voltage (Vt) from the x-intercept and a mobility-related slope (m). Since $m \propto \sqrt{\mu_{eff}}$, we utilize m^2 as a proxy for intrinsic mobility. Finally, the external parasitic resistance (Rext) is determined from the y-intercept of the total resistance (Rtot = Vds/Id) plotted against 1/(Vgs–Vt).

This analysis confirms that Rext is a significant component, accounting for about 40% of the measured Rtot,in agreement with published literature for this node [6].

To isolate stress-induced mobility effects from Vt shifts, we adopted a constant-overdrive extraction method. Drive current Id was measured at a fixed gate overdrive voltage (Vov = Vgs – Vt = 0.3V), using the Vt extracted via Y-Function method. This approach is widely used in advanced CMOS characterization and variability studies [7].

TABLE I. Typical Parameters of 7nm FinFET Technology

Parameter	Value
Fin Pitch	30 nm
Fin width	6 nm
Fin height	40 nm
Gate length	16 nm
Poly pitch	56 nm
Number of fins	2 and 4 fins
Gate fill	Tungsten

III. Technology and Simulation Setup

Process and device simulations were carried out using the Synopsys Sentaurus TCAD 3D tool (version U-2022.12), employing a FinFET device model representative of a generic 7 nm foundry FinFET technology node and process assumptions. The key simulation parameters for the 7 nm silicon FinFET technology are summarized in Table I. The process simulator includes key fabrication steps—fin patterning, epitaxial source/drain growth, and contact formation—while tracking thermal history to capture stress evolution. Stress computation accounts for lattice mismatch in epitaxial regions and thermal expansion differences during tungsten fill. Electrical behavior was modeled by linking stress-induced mobility variations to drive current changes. Calibration was achieved using nominal reference structures and experimental data from dedicated test structures, ensuring consistency between simulated and measured performance trends. Details were described in [3].

In this technology, Sidewall-Assisted Double Patterning (SADP) is employed for gate definition [8,9], while Sidewall-Assisted Quadruple Patterning (SAQP) is used for fin patterning [10-11]. Both are standard techniques widely adopted by leading FinFET manufacturers due to their superior CD uniformity and low line edge roughness (LER). However, while the feature CD remains tightly controlled, the spacing between features is more prone to variability, primarily due to

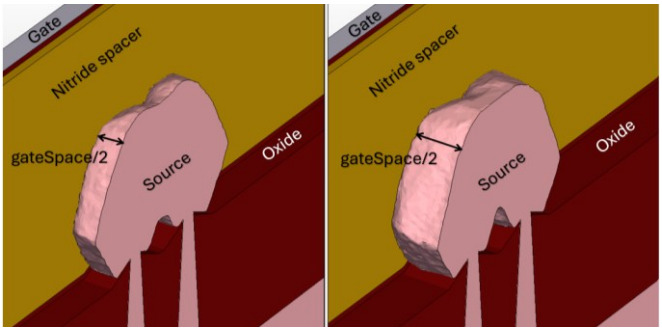

Fig.2 Simulated 3D structure (showing silicon, gate spacer, and silicon trench insulator oxide only) of devices with different poly space and the relative epitaxial growth shape

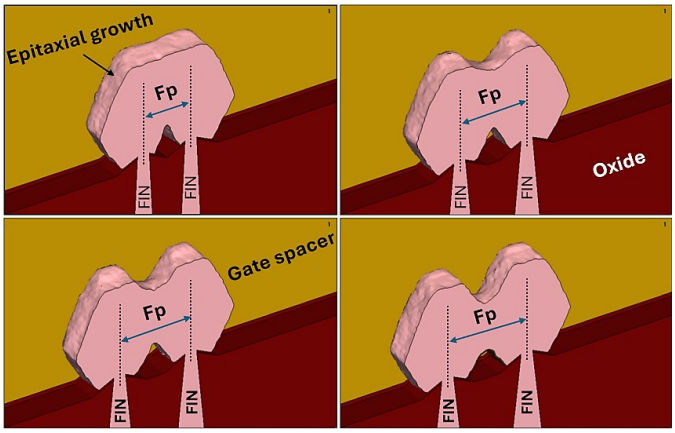

Fig.3 Simulated 3D structure (showing silicon, gate spacer, and silicon trench insulator oxide only) of devices with different fin pitches and the relative epitaxial growth shape

process-induced deviations in mandrel lithographic CD control. This variability in spacing is a key contributor to stress-induced performance changes in scaled devices.

The simulation model incorporates the major fabrication steps, from fin patterning through source/drain/gate (S/D/G) contact formation, while also tracking the thermal history across critical process stages.

To accurately model the epitaxial growth of the source/drain regions, the simulation includes an atomistic Lattice Kinetic Monte Carlo (LKMC) module [12]. This module enables high-fidelity modeling of the epitaxial deposition process, which is crucial for this study, as the poly and inter-fin spacing directly influences the volume and morphology of the grown material, and consequently, the stress state in the active regions.

Figs. 2-3 present the resulting 3D structures generated by the TCAD model, illustrating devices with varying poly pitches and fin pitches, respectively. These figures demonstrate how epitaxial growth differs in two-fin devices under different layout conditions. In both scenarios, the volume of the epitaxially grown source and drain regions changes, directly influencing the mechanical stress induced in the device channel. In the case of varying fin pitch (Fig.3), the change not only affects the volume but also alters the morphology of the stressors. As the fin pitch increases, the epitaxial regions tend to separate, transitioning from a merged to a more isolated diamond-like shape. This separation modifies both the magnitude and profile of the stress within the channel.

In this study, we simulated the mechanical stress profiles in the transistor channel as functions of both poly pitch and fin pitch. The resulting stress data were then used to model the impact on carrier mobility, thereby linking layout-induced stress modulation to variations in transistor performance. To protect the confidentiality of the particular foundry silicon process and the raw measurement data, we use normalized representative of typical data for performance modulation. The percentage difference is a common way of expressing performance degradation and a gap to the model.

Fig.4 shows the simulated stress distribution at the channel center. The left panel presents the longitudinal stress profile across the fin cross-section, while the right panel plots the

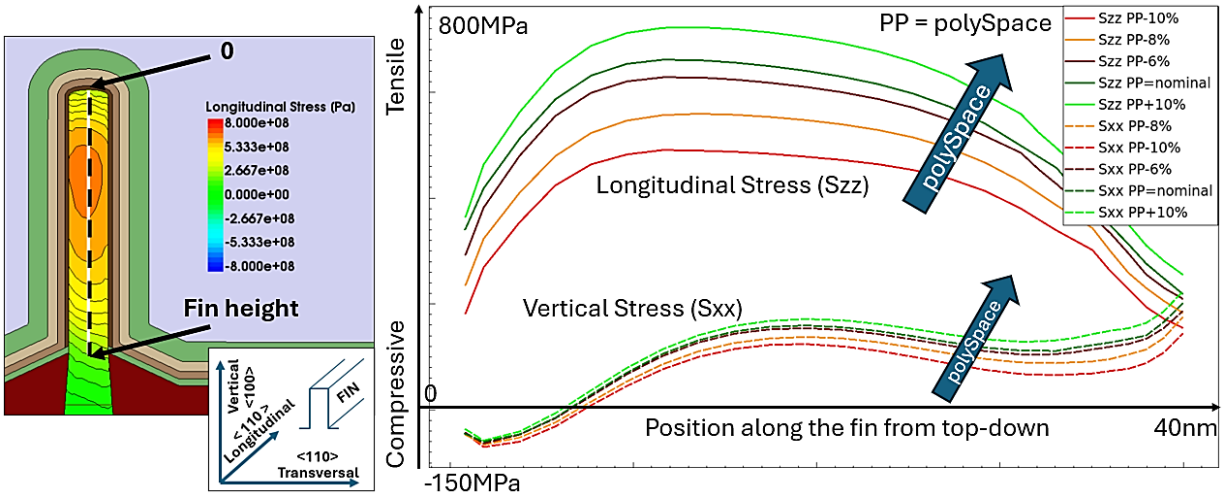

Fig. 4. Simulated stress profiles at the channel center in NMOS devices. Left: fin cross-section showing longitudinal stress distribution. Right: plot of vertical and longitudinal stress along the dashed section on the left for different poly pitches.

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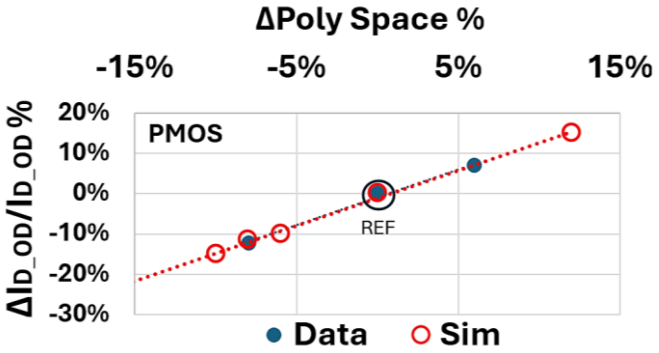

Fig.5 Experimental data and simulation of drain current change in linear region (@Vsd=0.05V) as a function of poly space for 2-fin PMOS devices

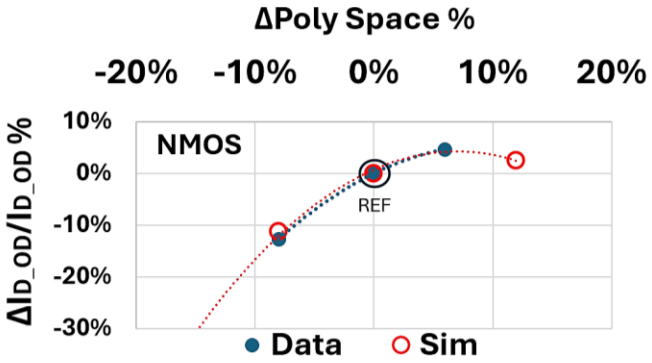

Fig.7 Experimental data and simulation of drain current change in linear region (@Vds=0.05V) as a function of poly space for 2-fin NMOS devices

vertical and longitudinal stress components along the indicated section for different poly pitch values. Because stress along the fin can exhibit complex local variations, as evident in Fig.4, this work reports stress values as averages integrated over the entire channel region.

IV. POLY PITCH EFFECT ANALYSIS

In SADP patterning, the poly CD is primarily determined by the spacer formed through a highly controlled Atomic Layer Deposition process on a backbone mandrel. However, variations in the mandrel CD introduced during lithography affect the spacing between adjacent poly lines. Therefore, this analysis focuses on changes in poly space rather than poly CD.

In advanced FinFET CMOS technologies, the source and drain regions of PMOS and NMOS transistors are grown epitaxially in a recessed cavity of the fin, between gate poly-Si lines. PMOS uses boron-doped SiGe while NMOS gets phosphorus doped Si. Since those process operations are performed in sequence, they can be optimized independently to meet distinct performance targets. Variations in the geometry or volume of these stressor regions modulate the stress level in the channel, thereby influencing carrier mobility and overall device performance.

We used constant-overdrive biasing to isolate mobility-driven effects from threshold variations. Since the Y-function extraction shows $\Delta Vt \leq 10–20$ mV among devices, as shown in Fig.9, sampling at fixed Vgs or at fixed Vov yields practically the same sensitivity. We report results at Vov = 0.3 V, and we verified that trends are unchanged at Vov = 0.2 V.

A. PMOS FinFET devices

Fig.5 illustrates the change in PMOS drain current in the linear region as a function of the poly space variation. The plot displays both the simulated electrical performance (open circles marked "Sim") and the measured electrical results on silicon (closed circles marked "Data"). As the poly spacing increases, PMOS performance improves linearly, showing a total change between -11% and +7% for a -8%/+6% change in poly spacing. This trend is expected, as a wider poly space increases the proportion of the SiGe-stressed region relative to the silicon channel, thereby enhancing hole mobility. This is further confirmed with simulation. Fig.6 shows the simulated variation of the three components of stress on the PMOS channel. The transversal and vertical components do not significantly change with the poly space, because the transversal cross-section of the stressors does not undergo substantial deformations. However, while Ge concentration remains constant, the volume of the SiGe source/drain stressor increases with poly spacing, inducing an increase in longitudinal stress and a resulting

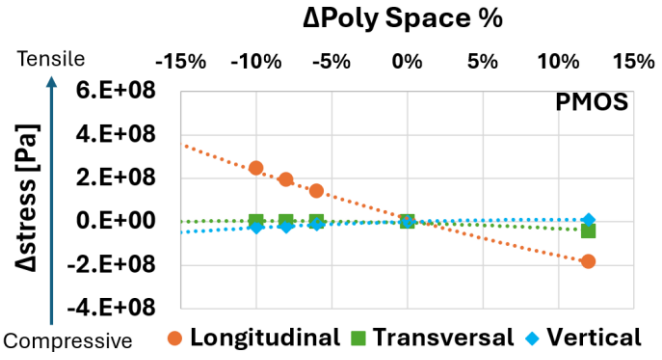

Fig.6 Simulated magnitude of stress components change as a function of the gate space for 2-fin PMOS transistor (reference device corresponds to the nominal poly space).

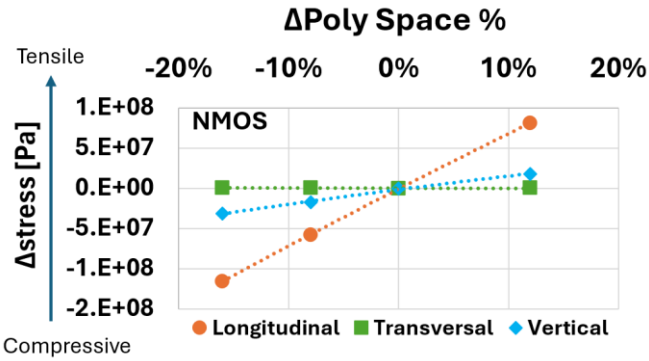

Fig.8 Simulated magnitude of stress components change as a function of the gate space for 2-fin NMOS transistor (reference device corresponds to the nominal poly space).

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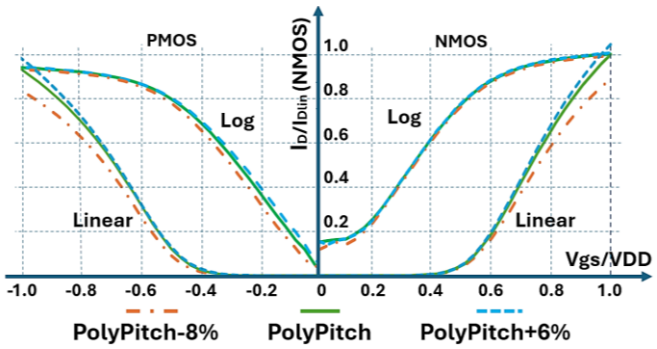

Fig.9 Normalized Id-Vgs characteristics for 2-fin PMOS (left) and NMOS (right) devices. Log-scale plots show negligible Vt shift (about 10mV for NMOS and 20mV for PMOS, as extracted). Linear-scale plots, showing clear modulation of channel slope (mobility). Current values are normalized to the max value of NMOS Id (Vgs=VDD; Vds=50mV)

performance improvement. Normalized Id-Vgs data is presented in Fig. 9. The log-scale plot confirms that the Vt shift induced by poly space variation is limited to ~20mV for PMOS. The modulation of the S/D volume impacts both intrinsic mobility and parasitic resistance. Our de-embedded analysis described in Section II confirms that Rext varies significantly (Fig.10 top, up to +30% for PMOS), and the intrinsic mobility proxy (Fig. 10 bottom) shows a clear positive trend (from -23% to +11%), confirming that the performance gain is driven by stress-enhanced mobility.

B. NMOS FinFET devices

Fig.7 illustrates the change in NMOS drain current in the linear region as a function of the poly space. The performance gradually increases with larger poly space, but the sublinear behavior suggests a more complex stress interaction when compared to the PMOS case. The performance change is between -13% and +5% for a -8%/+6% change in poly space.

The analysis of stress components is shown in Fig.8. The longitudinal component, and to a lesser extent, the vertical component, increase linearly with the poly space. The overall effect on mobility is dominated by the longitudinal component, linearly enhancing device performance. In contrast, despite the vertical component having a more contained variation, it has a more pronounced effect on electron mobility [1], inducing a sublinear trend in the current, as shown in Fig.7.

Fig.9 (log scale) shows that the threshold voltage shift is minimal (the extracted value is ~11 mV for NMOS), so Vt variation is not the main contributor. In contrast, the linear-scale plot reveals a clear change in the slope of the Id-Vgs curve, pointing to mobility as the dominant factor.

We analyzed the impact of various factors contributing to the change in characteristics and summarized the result in Fig.10. The top panel shows the contribution of the parasitic resistance (Rext), which changes significantly (due to S/D volume change), up to +18% for NMOS. The bottom panel isolates the intrinsic effect: the mobility proxy parameter (m^2) follows its own trend, from −23% to +2%, independent of Rext.

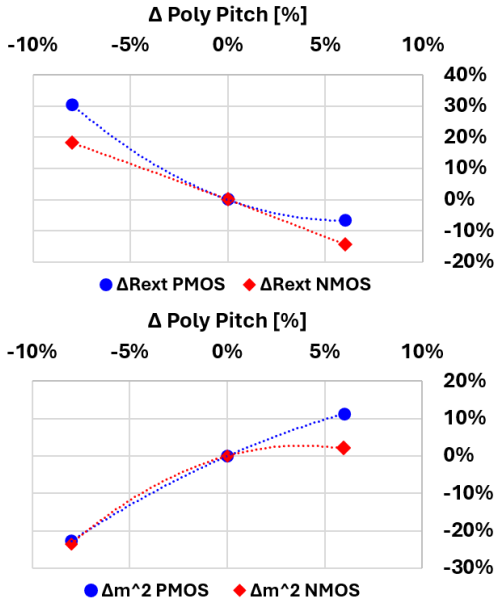

Fig. 10. (Top) Percent variation of extracted parasitic resistance (ΔRext %) and (Bottom) percent variation of intrinsic mobility proxy (Δm^2 %) as a function of ΔPoly Space for NMOS and PMOS devices, from the Y-Function de-embedding.

These findings demonstrate that, even after accounting for Rext variation, the main mechanism behind the performance trend in Fig.7 is the modulation of intrinsic channel mobility, consistent with the stress patterns predicted in Fig.8.

Since compressive stress degrades electron mobility, SiGe is not used for NMOS source/drain regions. Instead, NMOS devices typically utilize silicon epitaxy, which introduces minimal stress and maintains favorable electron transport characteristics. Consequently, the causes of stress variations must be sought in a different process step other than epitaxial S/D growth.

In NMOS devices, stress modulation is primarily driven by tungsten contact deposition rather than S/D epitaxy. To capture this effect, the TCAD model includes a thermo-mechanical simulation step after tungsten fill, assuming deposition at 450 °C followed by cooling to 25 °C. The stress tensor is computed based on the thermal expansion mismatch between tungsten and silicon, using linear elastic constants for both materials. Poly pitch variation alters the contact area between tungsten and silicon, which changes the magnitude of tensile stress transferred to the channel.

In contrast, for PMOS devices, the stress impact from tungsten is relatively minor compared to the dominant influence of SiGe-induced stress. This tungsten-induced stress mechanism was previously demonstrated and exploited in early planar Replacement Metal Gate (RMG) technology to enhance NMOS performance [13]. Residual tensile stress from tungsten fill was previously reported to modulate channel strain in FinFETs [14-15].

The observed changes in drive current are very significant for both NMOS and PMOS. In order to avoid high variability

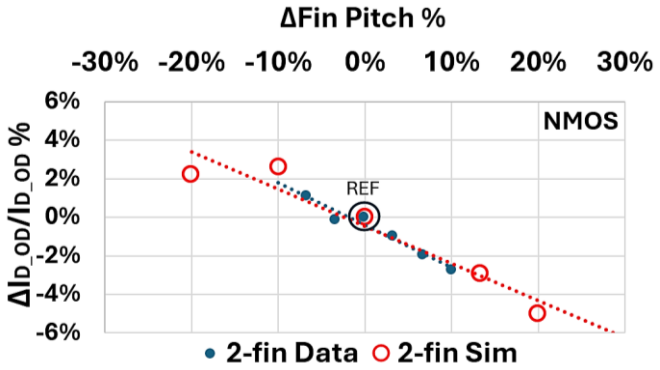

Fig.11 Experimental data and simulation of drain current change in linear region (@Vds=0.05V) as a function of fin space for 2-fin NMOS devices

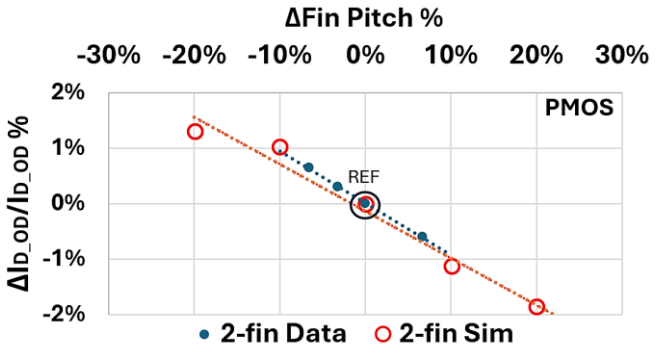

Fig.13 Experimental data and simulation of drain current change in linear region (@Vsd=0.05V) as a function of fin space for 2-fin PMOS devices

of devices and negative impact on product performance, the process control needs to ensure low variability of the poly pitch.

V. Fin Pitch Effect Analysis

Variations in fin space cause changes in the volume of epitaxial growth, but unlike the case of poly space, there is also a significant variation in its shape, as shown in Fig.3. This can cause a modification of the stress profiles in the device channel, therefore, it is important to analyze all three stress components to understand their combined effect on performance.

A. NMOS FinFET devices

Fig.11 illustrates the variation in NMOS drain current in the linear regime as a function of fin pitch (Fp). The plot includes both simulated electrical performance (open circles labeled "Sim") and measured silicon data (closed circles labeled "Data").

The experimental results show a linear dependence of the NMOS drive current within a ±10% variation in Fp, corresponding to approximately a 2% change in current. The simulation results extend this linear trend to a broader range of ±20%, confirming the consistency of the observed behavior.

To confirm this trend is intrinsic, we applied the same de-embedding methodology described in Section II. The analysis revealed that, unlike the poly pitch case, the variation in parasitic resistance (Rext) as a function of Fin Pitch was negligible (less than 2%). The intrinsic mobility proxy (m^2), however, was found to track the measured Id trend (Fig. 11) almost perfectly. This robustly confirms the performance change is driven by mobility modulation, not parasitic artifacts.

Fig.12 presents the simulated stress components in the NMOS FinFET channel as a function of fin pitch. As Fp increases beyond the nominal value, the volume of the epitaxially grown stressor regions also increases, resulting in a gradual increase in longitudinal compressive stress. The other stress components exhibit negligible influence on carrier mobility in this regime. Conversely, when Fp is reduced below the nominal value, the source and drain epitaxial regions merge (as shown in Fig.3, top-left), inducing a significant vertical compressive stress component, which has a dominant impact on electron mobility [1].

Simulations show that the transverse stress component has little influence on carrier mobility. However, the longitudinal and vertical components affect mobility in opposite way, partially offsetting each other's impact. Overall, the stress-induced impact on NMOS performance manifests as a gradual degradation in drive current with increasing fin pitch.

The agreement between simulation and experimental data

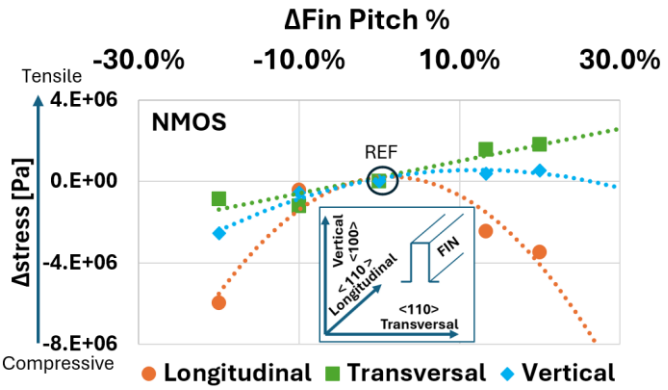

Fig.12 Simulated magnitude of stress components change as a function of the fin pitch for 2-fin NMOS transistor (reference device corresponds to the nominal fin pitch).

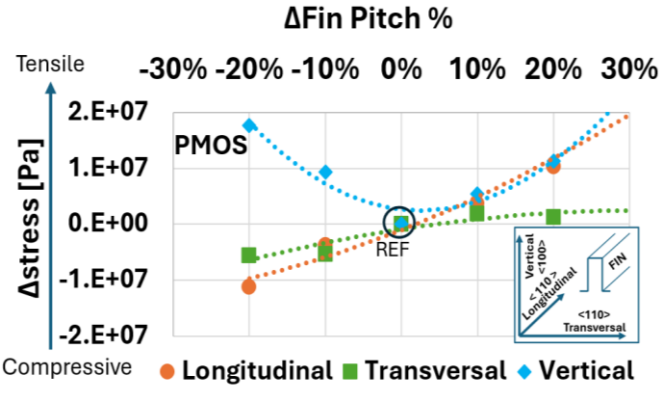

Fig.14 Simulated magnitude of stress components change as a function of the fin pitch for 2-fin PMOS transistor (reference device corresponds to the nominal fin pitch).

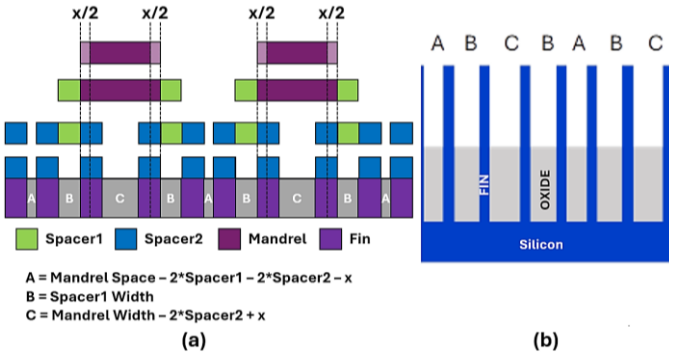

Fig.15 (a) SAQP pattern propagation sequence, from the top: Mandrel lithography (purple) with CD variability (x), first spacer deposition (green), second spacer deposition (blue), final Fin placement (violet); (b) sketch of fins showing variability of inter-fin space (fin "pitch walking") as shown in [10]

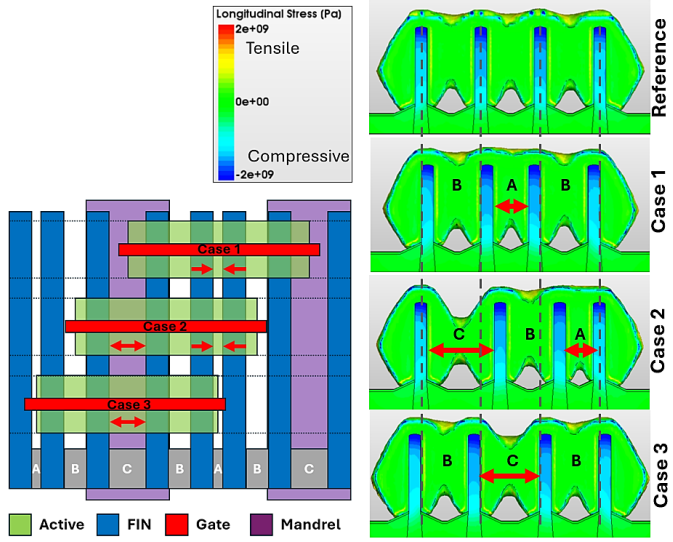

Fig.16 Positions in the sea of fins of a 4-fins device relative to the mandrel (left); Simulated cross section across the channel of 4-fins PMOS (right) with in blue the longitudinal compressive stress, for the three possible cases 1, 2, and 3

confirms that the observed degradation in transistor performance is primarily driven by stress variation resulting from the increase in inter-fin spacing.

B. PMOS FinFET devices

PMOS FinFETs benefit from enhanced performance due to longitudinal compressive stress introduced by SiGe source/drain stressors. However, variations in the geometry or volume of these stressors - driven by changes in fin pitch (Fp) - can significantly alter the stress distribution, making PMOS devices more susceptible to such variations than their NMOS counterparts. Fig. 15 presents both experimental and simulated data showing a monotonic degradation in PMOS drain current (in the linear regime) with increasing Fp. A ±10% variation in Fp results in an approximate ±1% change in current.

Fig. 14 illustrates the simulated stress components within the PMOS channel as a function of Fp. For positive Fp deviations, vertical compressive stress increases, which tends to enhance carrier mobility; however, this benefit is offset by a reduction in longitudinal compressive stress. Conversely, for negative Fp deviations, longitudinal stress becomes negligible, and the vertical and transverse components dominate, with the vertical component exerting a slightly stronger influence on mobility. The use of SiGe in PMOS amplifies stress-induced performance variations by nearly an order of magnitude compared to NMOS devices, which typically use Si S/D. Although vertical stress exhibits greater variation than longitudinal stress, it does not solely govern the mobility response.

Consequently, PMOS devices exhibit a reduced sensitivity to inter-fin spacing variations relative to NMOS devices. The strong correlation between simulation and experimental results confirms that the observed performance trends are primarily driven by stress modulation induced by fin pitch variation.

Table II summarizes the impact of variations in fin pitch and poly pitch on the linear drain current of NMOS and PMOS FinFET devices. The table presents the percentage change in current for each device type under specified pitch variation ranges. This table highlights that PMOS devices are more sensitive to poly pitch, while NMOS devices show greater sensitivity to fin pitch, though the overall variation is modest in both cases.

VI. Spacer-Assisted Quadruple Patterning

The most common fin patterning technique employed in advanced FinFET technology nodes is the Sidewall-Assisted Quadruple Patterning (or Self-Aligned Quadruple Patterning) (SAQP) [16]. Fig.15a illustrates the SAQP principle and highlights the impact of mandrel critical dimension (CD) variability (denoted by x, exaggerated for illustration purposes). A sketch of the cross-sectional view of the fins in Fig.15b shows the resulting variation in fin-to-fin spacing caused by mandrel CD errors.

Mandrel width variability leads to a phenomenon known as fin pitch walking, wherein the spacing between adjacent fins changes while the total width across four consecutive pitches remains constant, as schematically shown in Fig.15b. Understanding the impact of pitch walking on device performance is essential for evaluating stress-induced performance changes in scaled technologies.

The sensitivity of 2-fin and 4-fin devices, (typical device

TABLE II. Fin and Poly Pitch Impact on Linear Drain Current

Experiment	Pitch change	NMOS	PMOS
Fin Pitch	-7% +7%	+2% -2 %	+1% -1%
Poly Pitch	-8% +6%	-13% +5%	-11% +7%

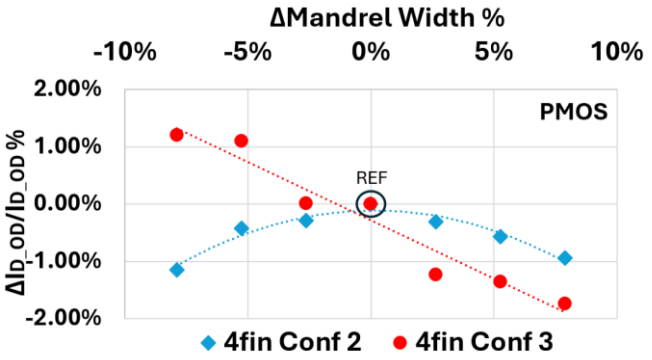

Fig.17 Experimental data of the linear drain current change as a function of Fin Pitch for 4-fin PMOS positioned in cases 2 and 3

sizes in 7 nm standard cell libraries) to pitch walking can vary significantly. In 2-fin devices, modulation is related to a single inter-fin space, as previously discussed in the context of variable fin pitch. In contrast, 4-fin devices may exhibit more complex behavior depending on their placement within the originally patterned fin array.

Fig.15 defines three pitch-walk parameters of interest (spaces A, B, and C), which are directly influenced by lithographic precision in mandrel width. The error in mandrel CD (x) introduces a mismatch between spaces A and C, as shown in the schematic and also shown in the cross-sectional view in Fig.15b.

By design, single-fin devices are immune to fin pitch walking. In 3-fin devices, only one inter-fin space is affected, rendering them relatively insensitive. However, the impact on 4-fin devices depends on their alignment relative to the SAQP mandrel, which defines their location within the uniform array of fins. Fig.16 illustrates three possible placements of a 4-fin device within the fin array. In the nominal case, all fin spaces are equal.

Based on the 2-fin model, closer fin proximity enhances epitaxial growth efficiency, thereby improving device performance. Consequently, Cases 1 and 3 exhibit monotonic but opposite performance trends due to mandrel-induced variations affecting the central fin spacing in opposite directions (refer to formulas in Fig.15). Case 2, by contrast, exhibits a parabolic response, as the lithographic error x symmetrically affects two fin spaces within the device.

Fig.17 presents the performance variation of a 4-fin PMOS device as a function of mandrel width error for Cases 2 and 3. The results confirm the analytical predictions, demonstrating that Case 3 is inherently less sensitive to fin pitch walking due to its symmetrical layout configuration.

VII. Applicability to Gate-All-Around Devices

The methodology presented in this work is expected to remain applicable to next-generation Gate-All-Around (GAA) nanosheet transistors; however, the underlying model parameters will require extensive recalibration. This is primarily due to fundamental structural and process differences between bulk-type FinFETs and GAA architectures [17]. In FinFET devices, the fin is a continuous extension of the substrate, resulting in a rigid monocrystalline structure, in which the lattice deformation in one region propagates elastically to the channel. In contrast, GAA devices employ multiple nanosheets that become separate crystal entities during the release process, resulting in rather complex strain coupling between nanosheets, interlayered with dielectric and metal fill.

Furthermore, the amount of longitudinal stress generated in the channel can be quite different in FinFET and in GAA nanosheet devices. In FinFETs, stress modulation is achieved by fin etch-back followed by epitaxial regrowth with materials of slightly different lattice constants, preserving a monocrystalline structure and enabling effective strain engineering. In GAA devices, source/drain regions form as separate epitaxial nodules that merge within the cavity, creating numerous crystal plane boundaries and dislocations. This reduces the strain contribution from lattice mismatch and makes stress highly dependent on the final crystal structure, dislocation density, and thermal history. Consequently, the amount of stress experienced by each nanosheet within the same device can vary, influenced by nanosheet dimensions, spacing, inter-sheet materials, and process conditions.

Accurate modeling for GAA devices will therefore require new formulations and detailed calibration against experimental data to capture these effects.

Conclusions

This study systematically investigated the impact of poly and fin pitch variations on mechanical stress modulation and electrical performance in 7nm FinFET devices. Through a combination of silicon measurements and TCAD simulations, we demonstrated that both NMOS and PMOS transistors exhibit sensitivity to layout-induced pitch changes, though the underlying mechanisms and magnitudes differ.

Poly pitch variations were found to significantly influence the volume of epitaxially grown source/drain regions, thereby modulating channel stress. PMOS devices, which utilize compressively stressed SiGe, showed a linear improvement in drive current with increasing poly space, reaching up to -11%/+7% variation. NMOS devices, in contrast, exhibited a more complex, sublinear response due to the interplay of longitudinal and vertical stress components, with performance changes ranging from -13% to +5%. A rigorous Y-Function de-embedding confirmed that while parasitic resistance varies significantly with poly pitch, the dominant driver for this performance change is the modulation of intrinsic channel mobility, not parasitic artifacts. The observed changes are significant enough to impact the performance of a product. Therefore, the poly-to-poly space needs to be controlled in a very tight manner.

The magnitude of the effects observed in our work are consistent with reported sensitivity ranges in studies from the industry, where local layout effects and process variability can

induce 5–20% performance shifts in advanced FinFET nodes [18].

Fin pitch variations also affected stress profiles, particularly through changes in epitaxial morphology. NMOS devices showed a modest ±2% current variation for ±7% fin pitch changes, while PMOS devices were less sensitive, with only ±1% variation. These effects were further compounded in multi-fin configurations due to pitch walking, a phenomenon inherent to SAQP-based patterning.

Overall, the results underscore the critical role of mechanical stress in determining FinFET performance and highlight the importance of precise pitch control in advanced CMOS technology nodes. The strong correlation between experimental data and simulation validates the modeling approach and provides a robust framework for future design and process optimization.

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